

Exploiting Half-Wits: Smarter Storage for Low-Power Devices

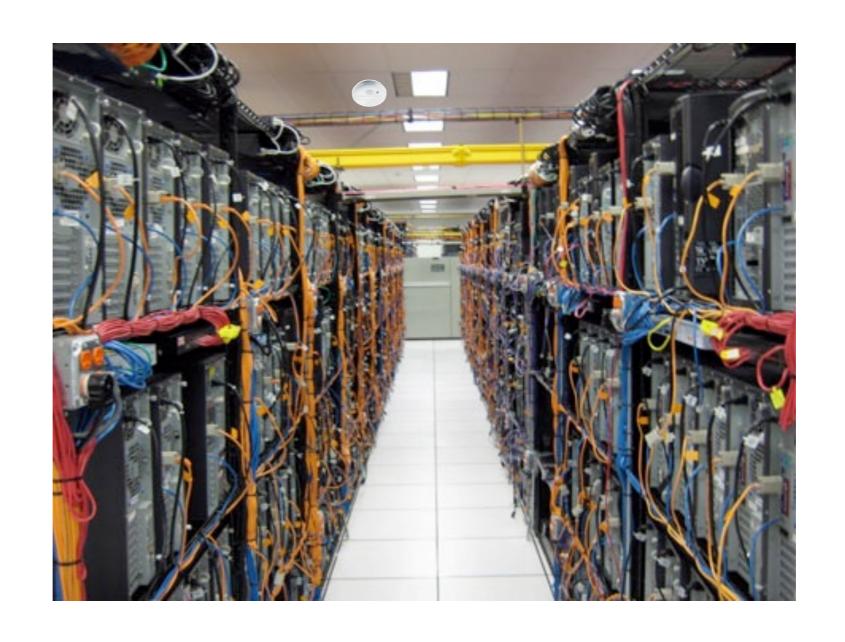


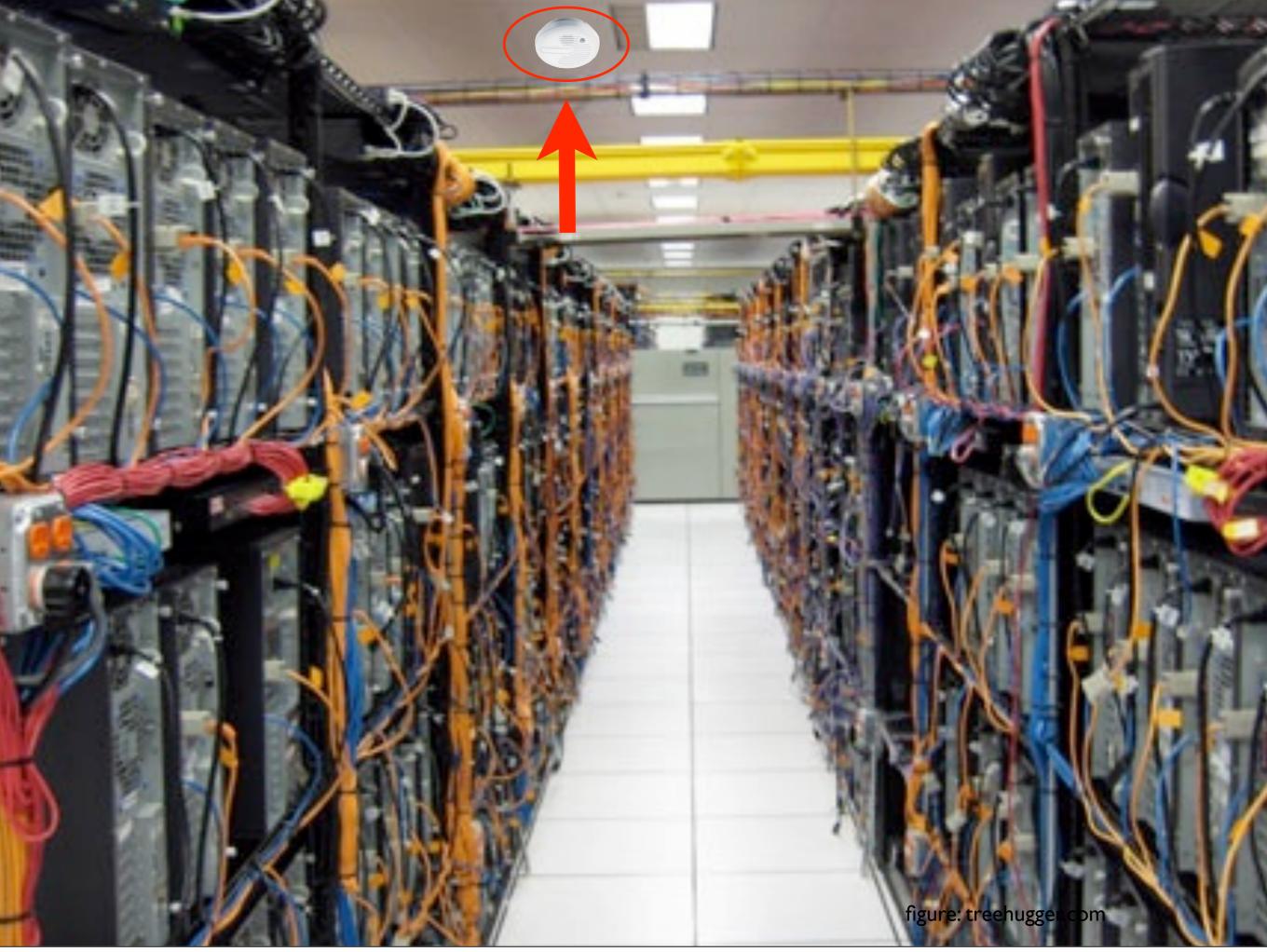
Mastooreh (Negin) Salajegheh, Yue Wang Kevin Fu, Andrew Jiang, Erik Learned-Miller



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Friday, March 4, 2011















On-chip Flash



On-chip Flash



Mastooreh Salajegheh, USENIX FAST 'I I

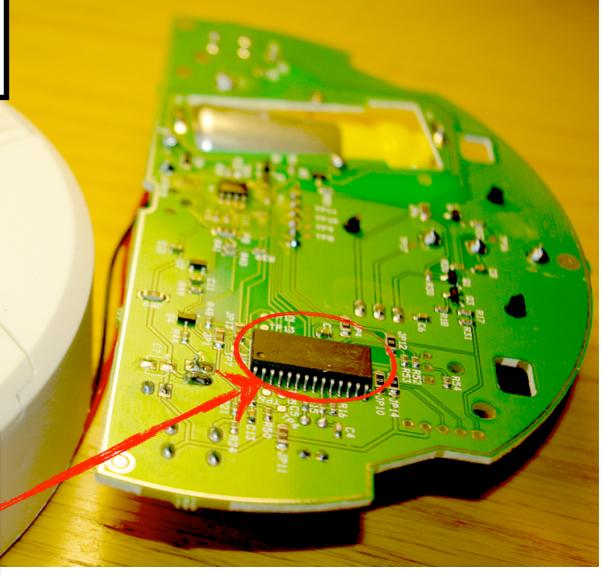


On-chip Flash

2.2 V vs. 4.5 V

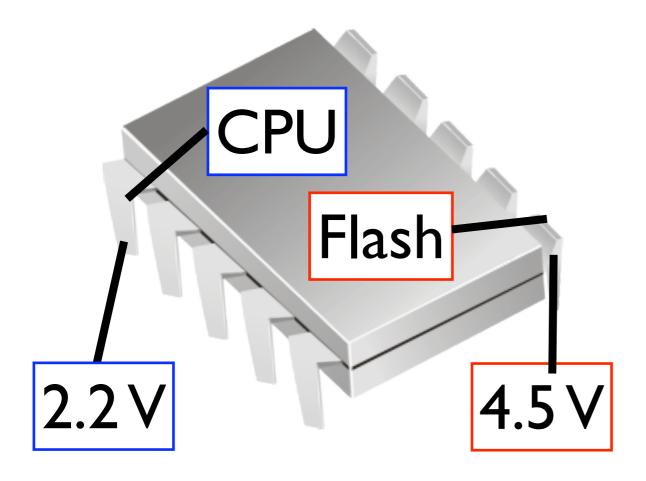


Microcontroller with 8KB Embedded Flash Memory





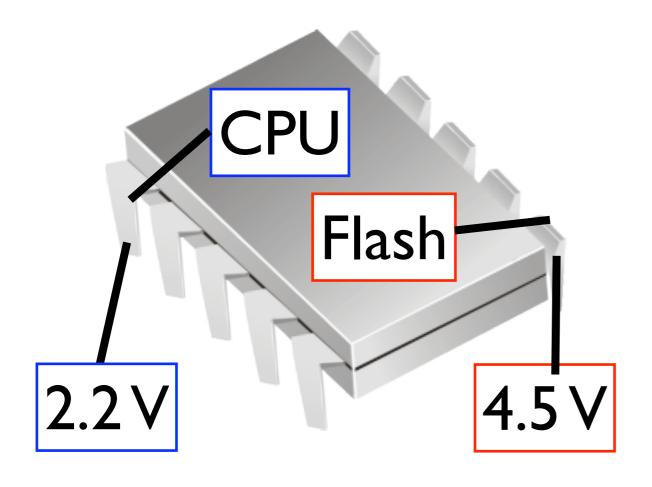
Ideal

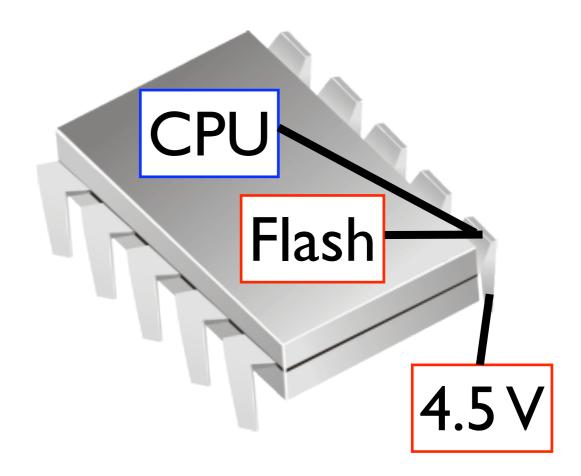


Energy ∝ Workload

Ideal

Actual





Energy ∝ Workload

Energy ∝ Worst case

Goal of this work

 To reduce the wasted energy consumption for embedded storage.

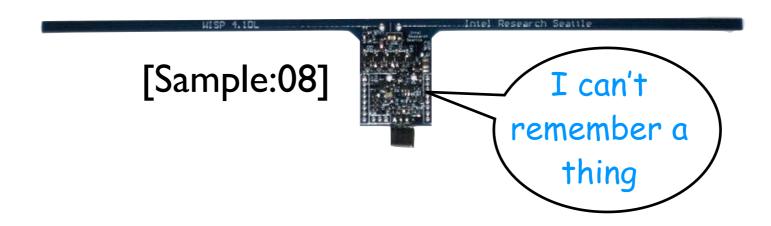
Contribution

- Software for using flash memory at low voltage
 - Quantifying the impact on reliability
 - Measuring the energy savings

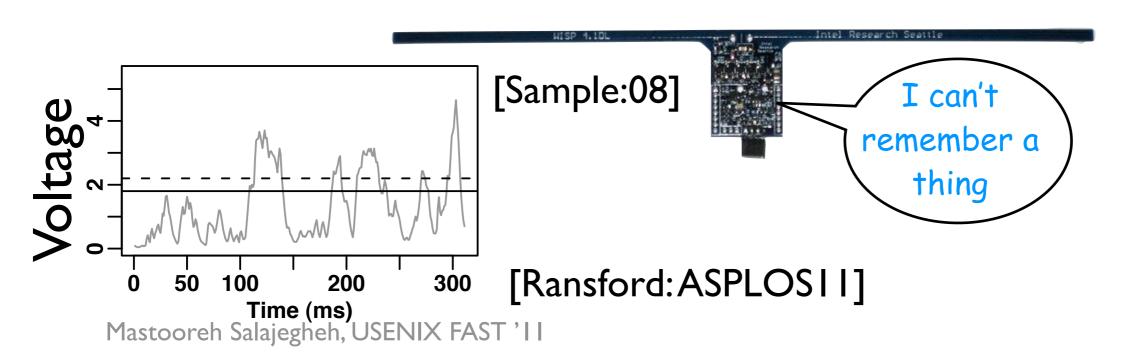
Pick the highest voltage...Excessive power

- Pick the highest voltage...Excessive power
- Add hardware...\$\$

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- Don't use flash memory...Ugh!



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Our Approach

Savings: Low-voltage

Write to flash memory at low voltage.

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How hard is it to correct the errors?



• Example:

Initialized:

• Example:

• Example:

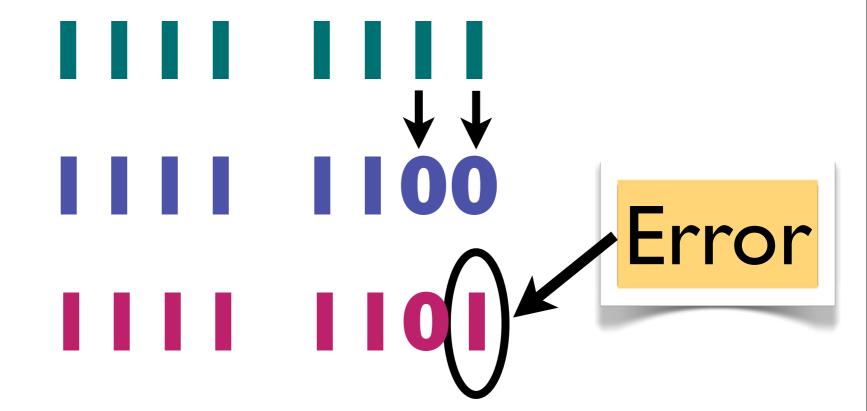
• Example:

• Example:

Initialized:

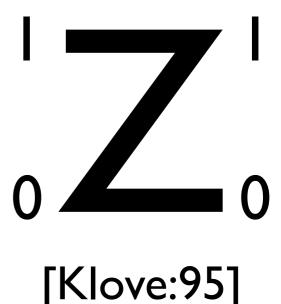
Input:

Result:



Transitions at low voltage

- $I \rightarrow 0$ might fail with $P \ge 0$.
- $I \rightarrow I$ never fails (P=0).



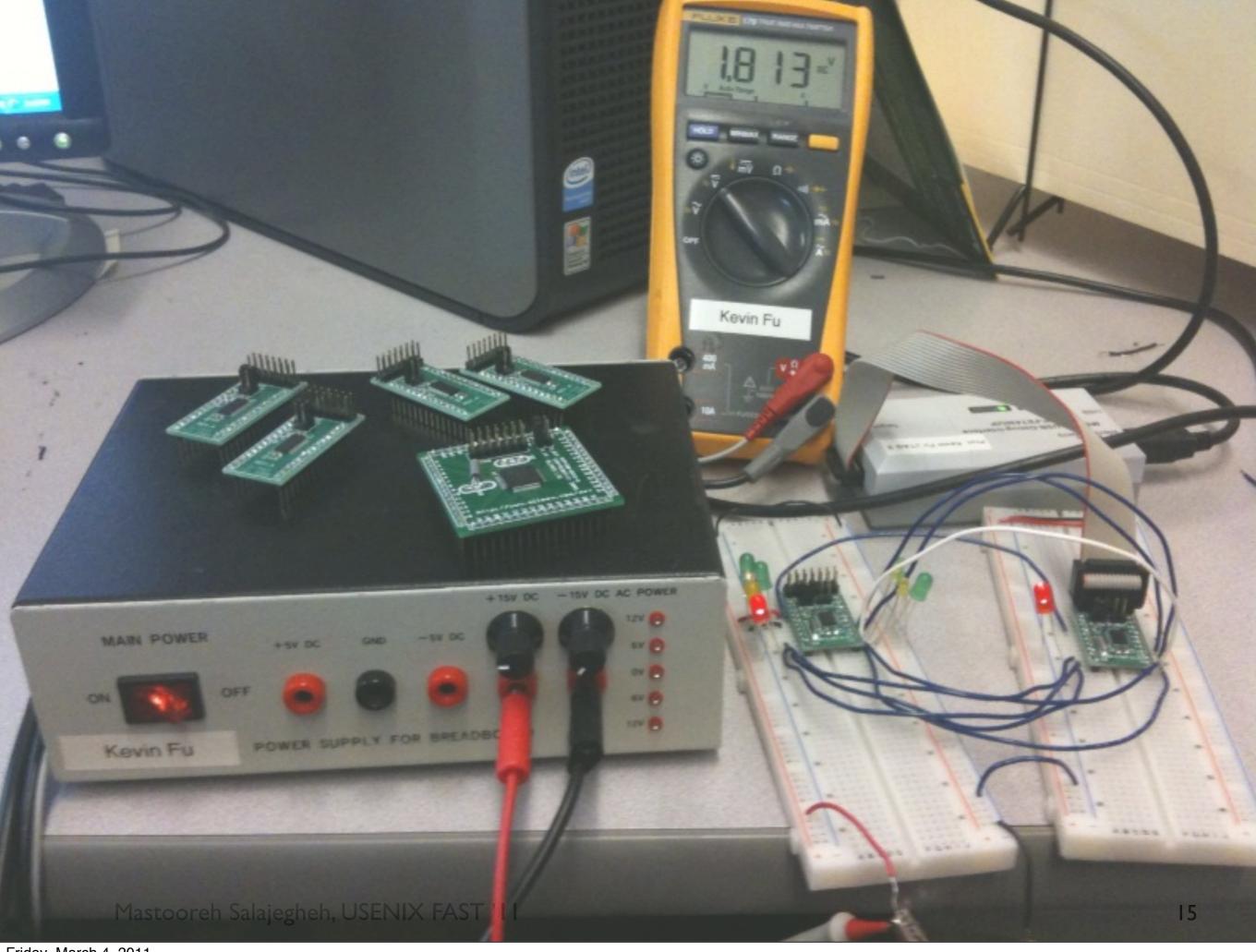
✓ Operating voltage level

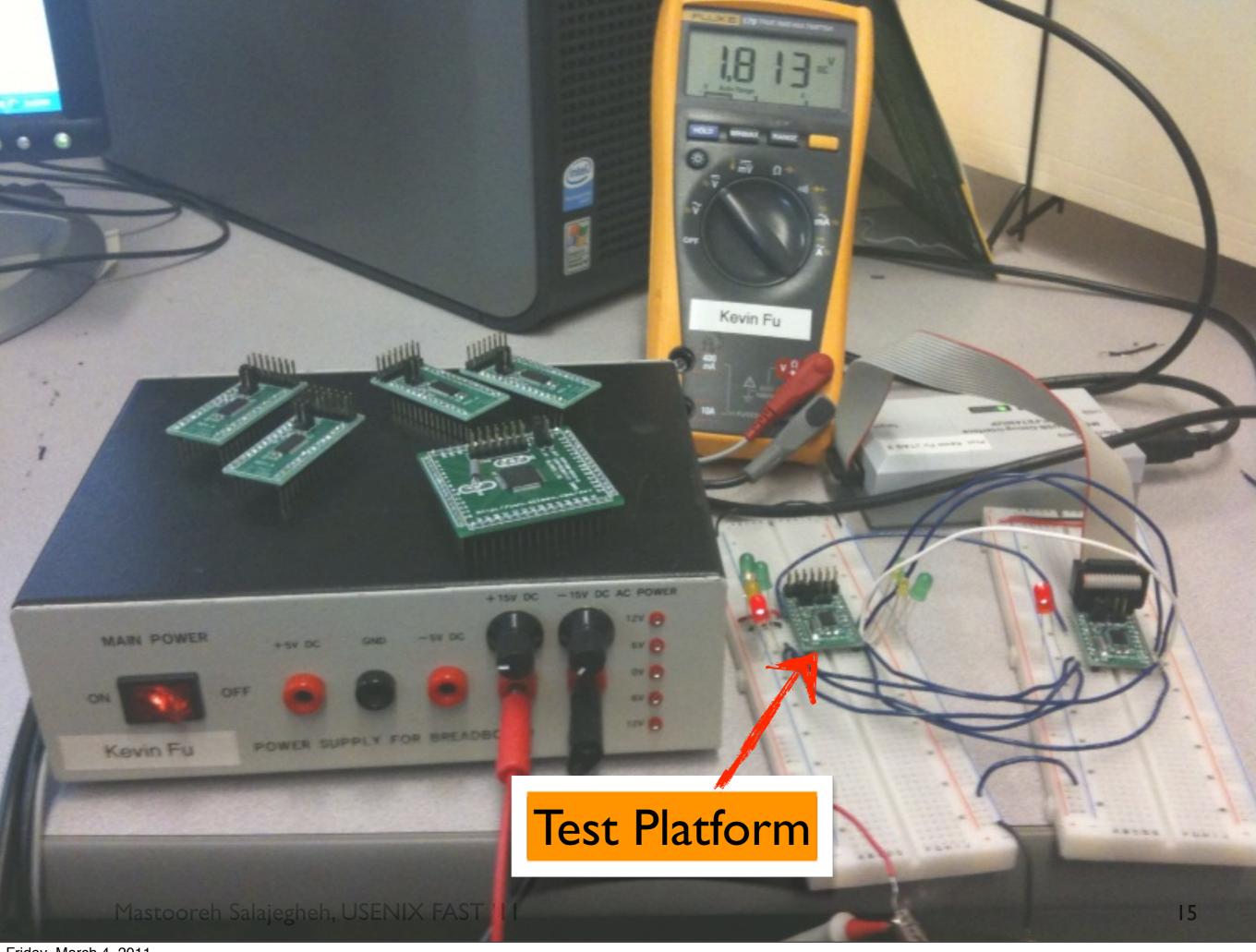
- ✓ Operating voltage level
- √ Hamming weight of data

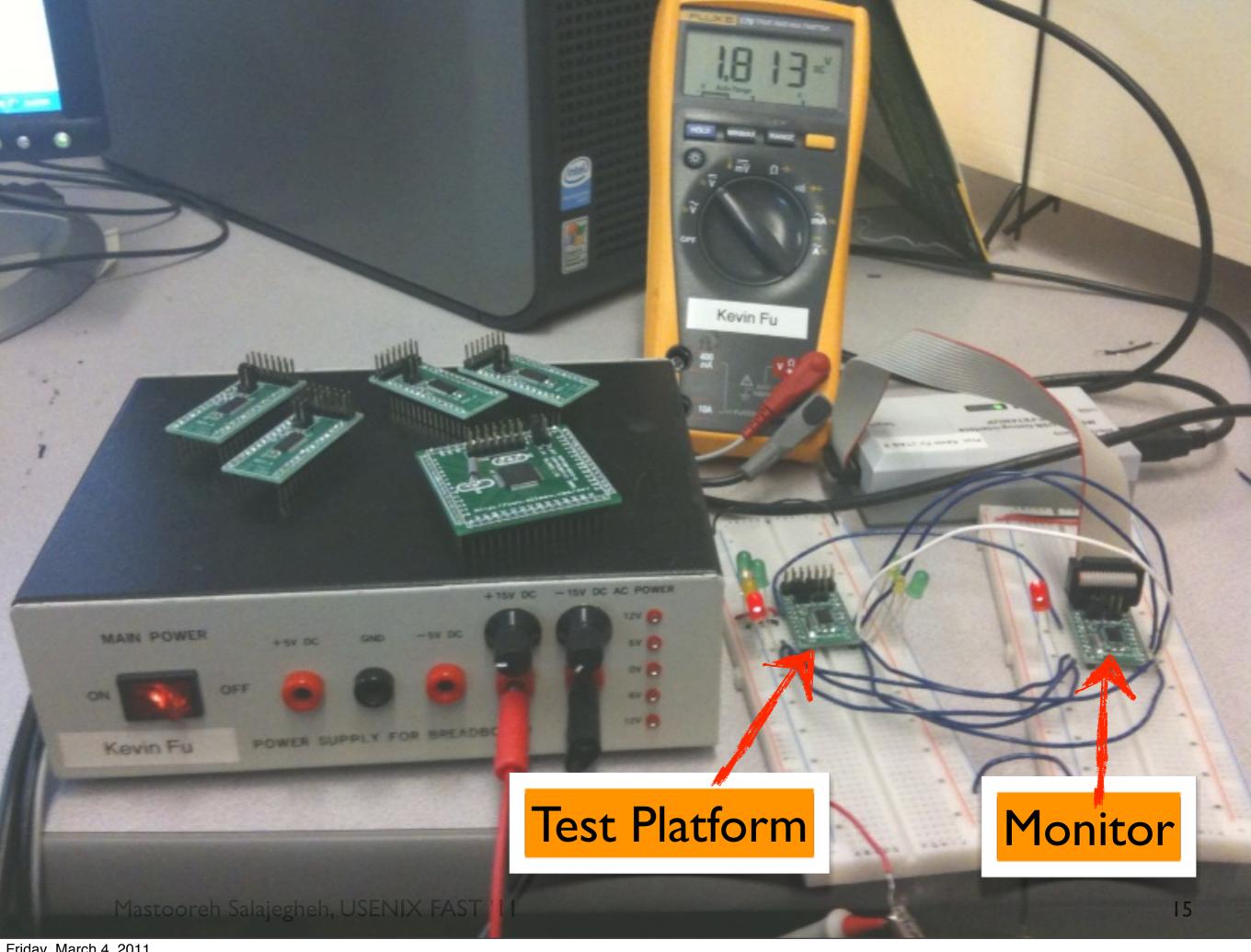
- ✓ Operating voltage level
- √ Hamming weight of data
- √ Wear-out history

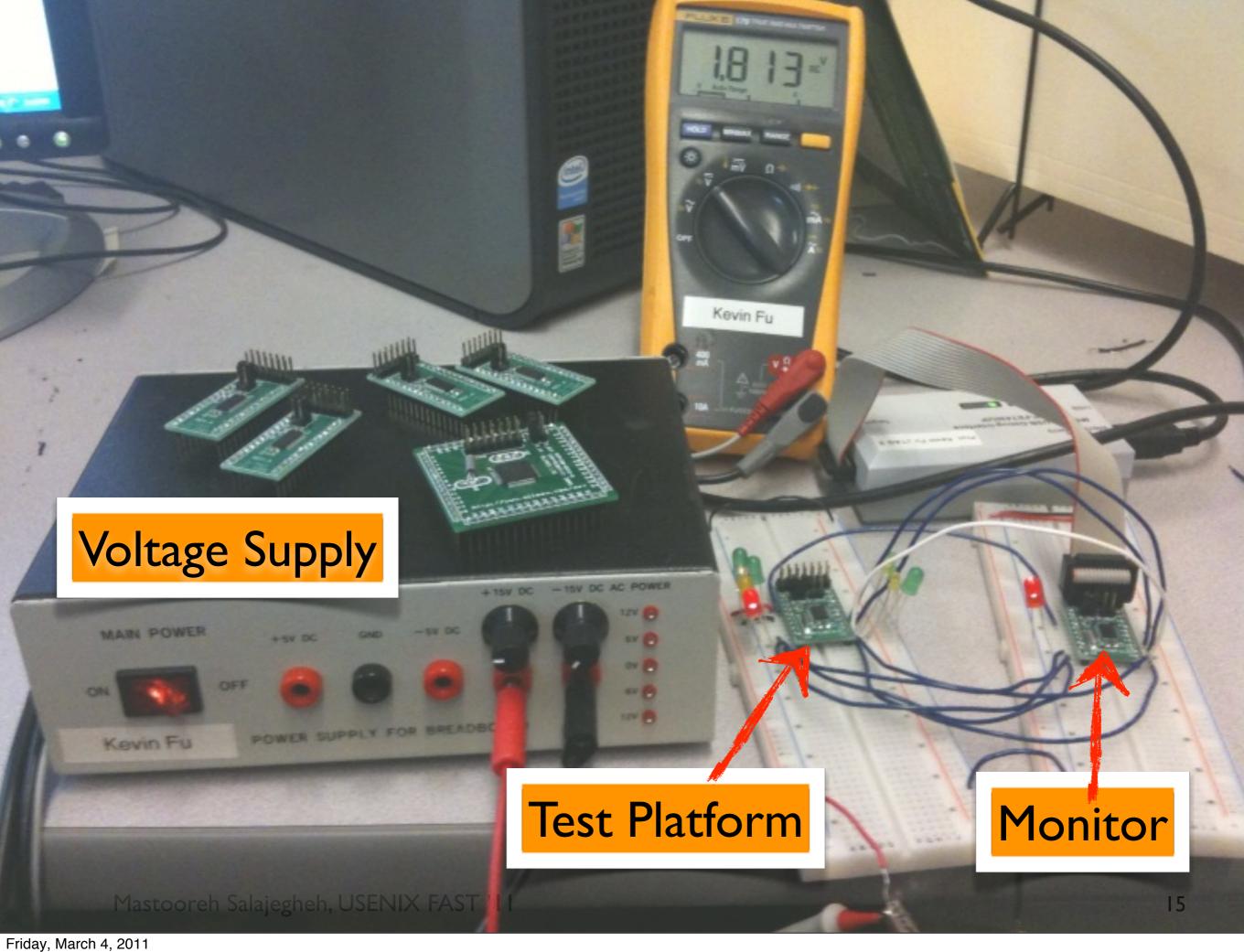
- ✓ Operating voltage level
- √ Hamming weight of data
- √ Wear-out history
- Neighbor cells

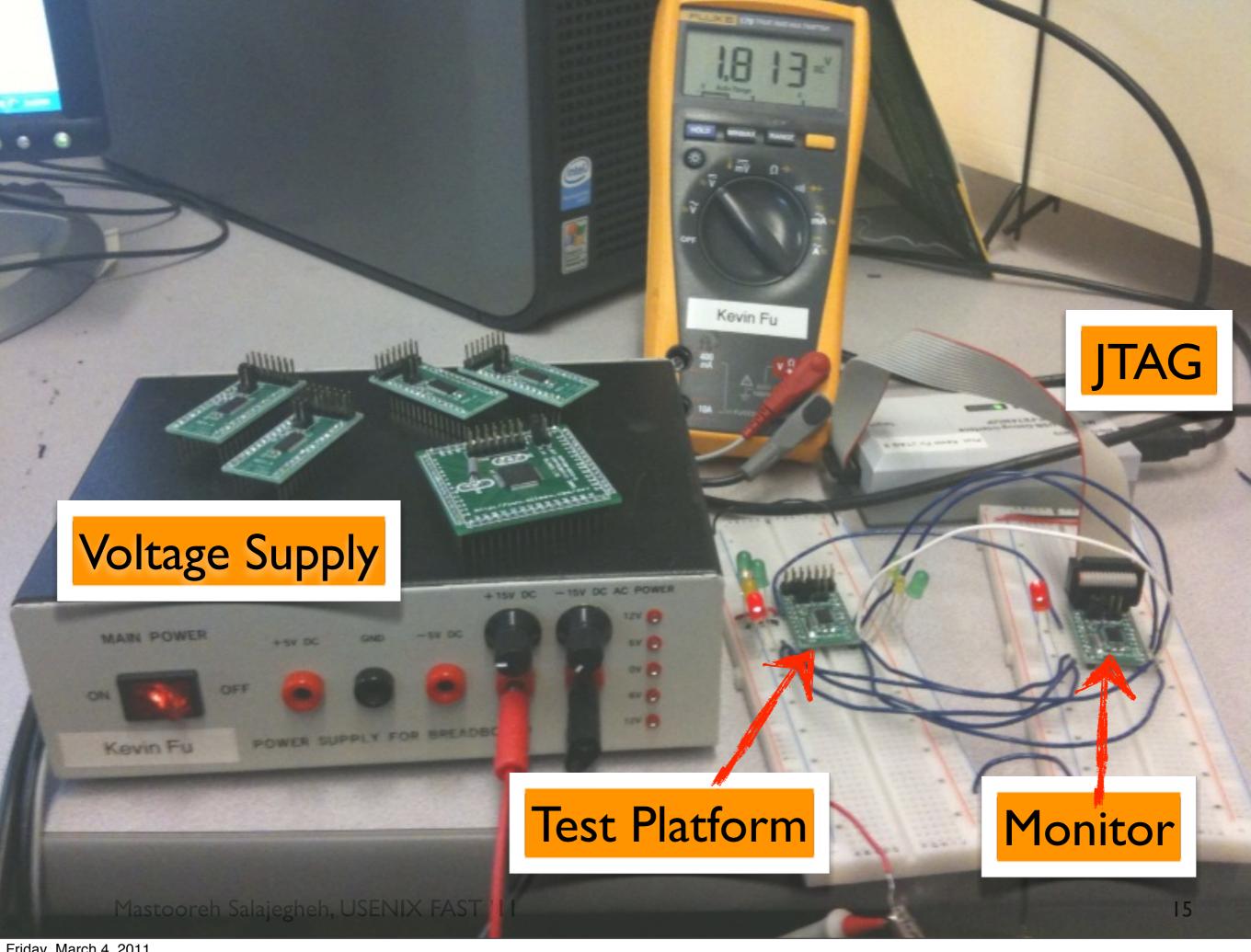
- ✓ Operating voltage level
- √ Hamming weight of data
- √ Wear-out history
- Neighbor cells
- Permutation of 0s

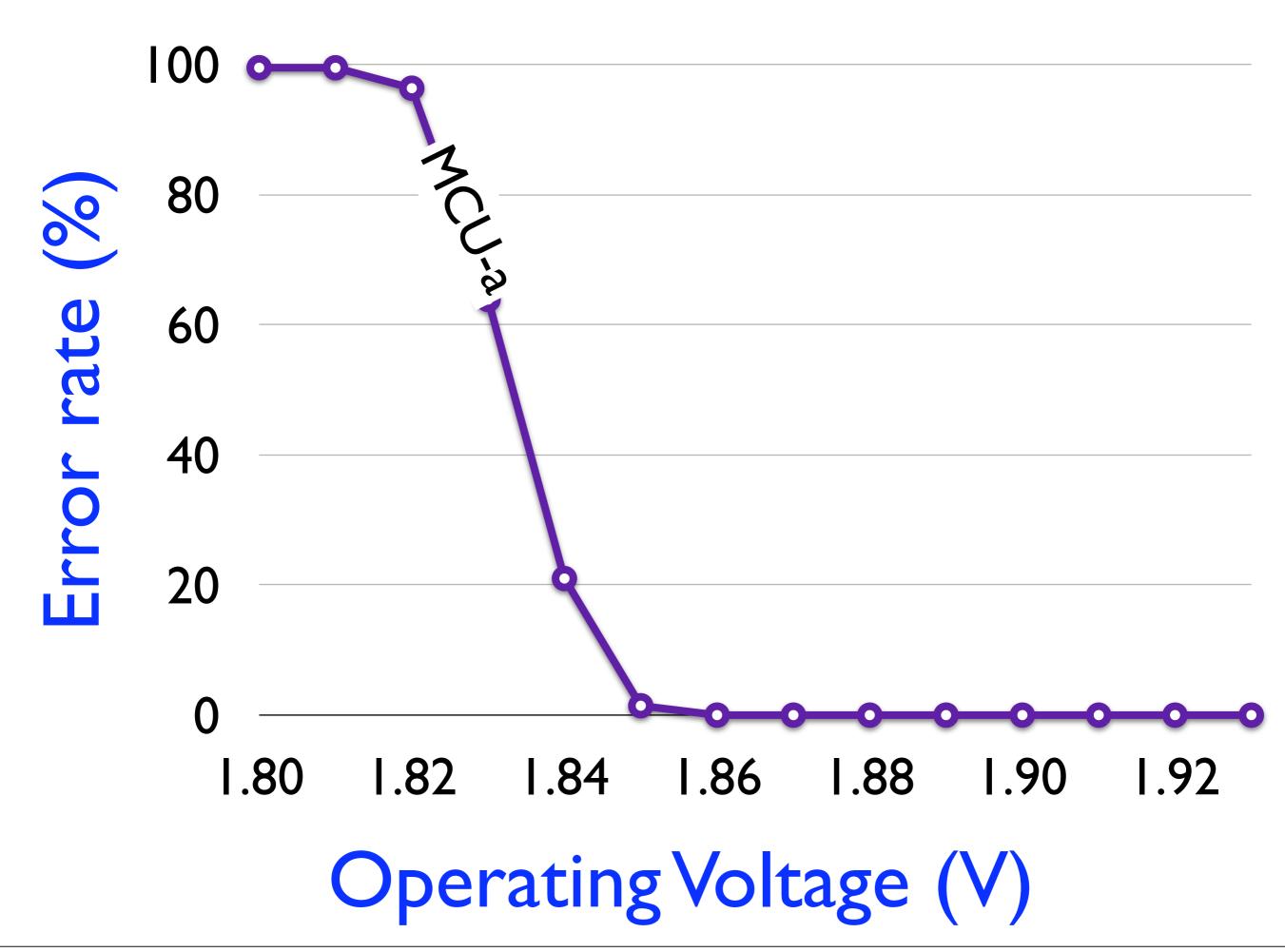


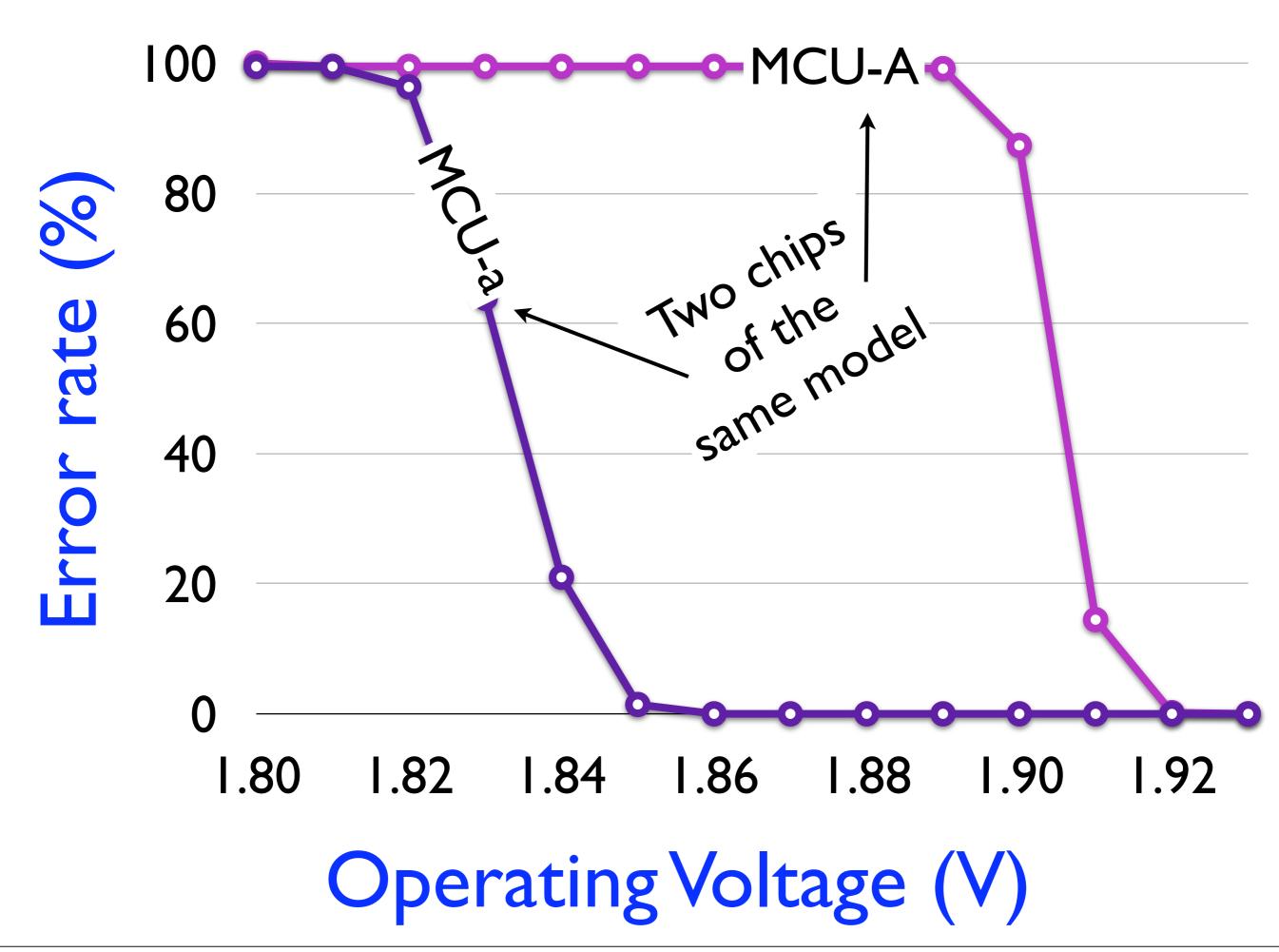


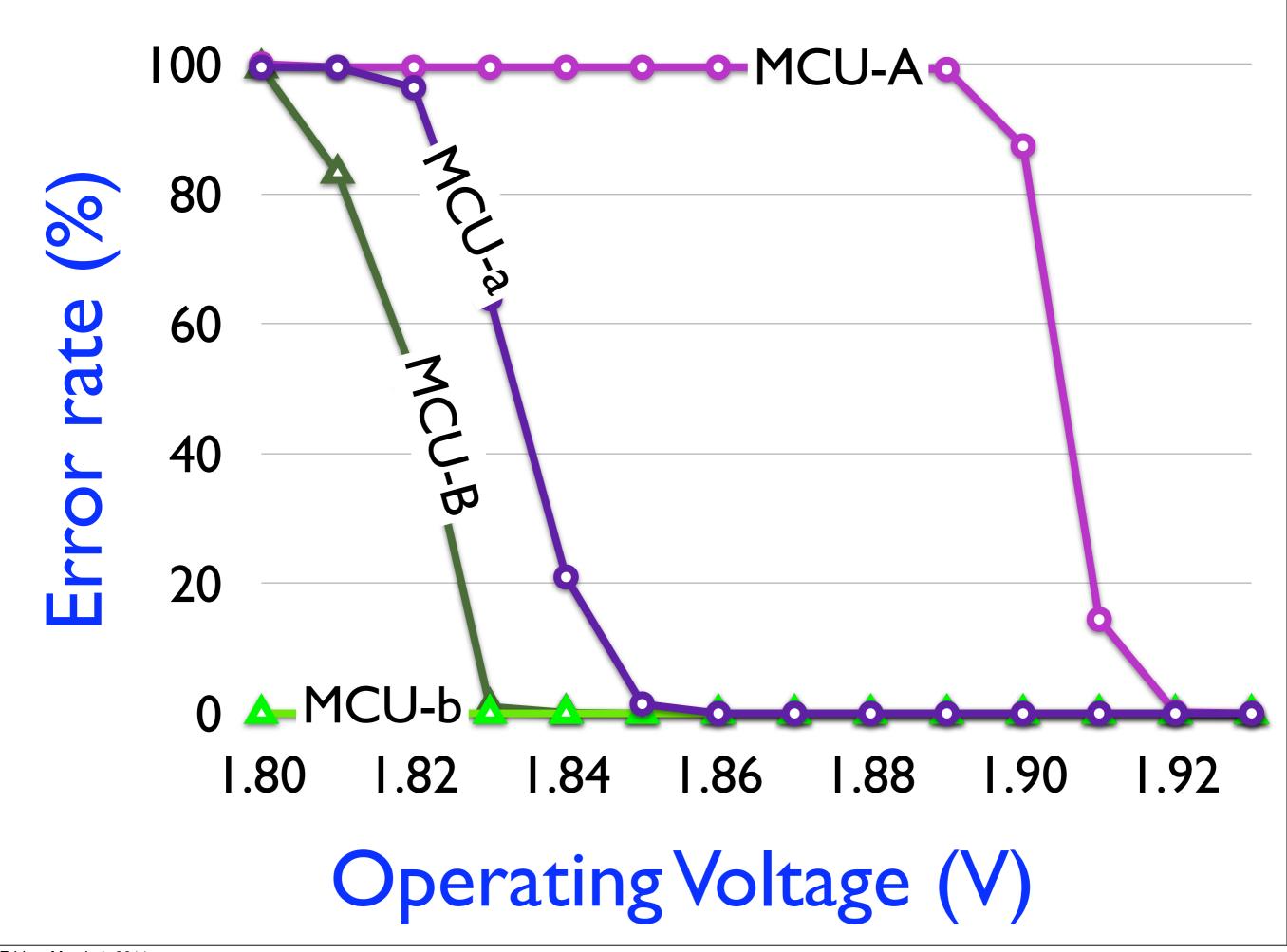




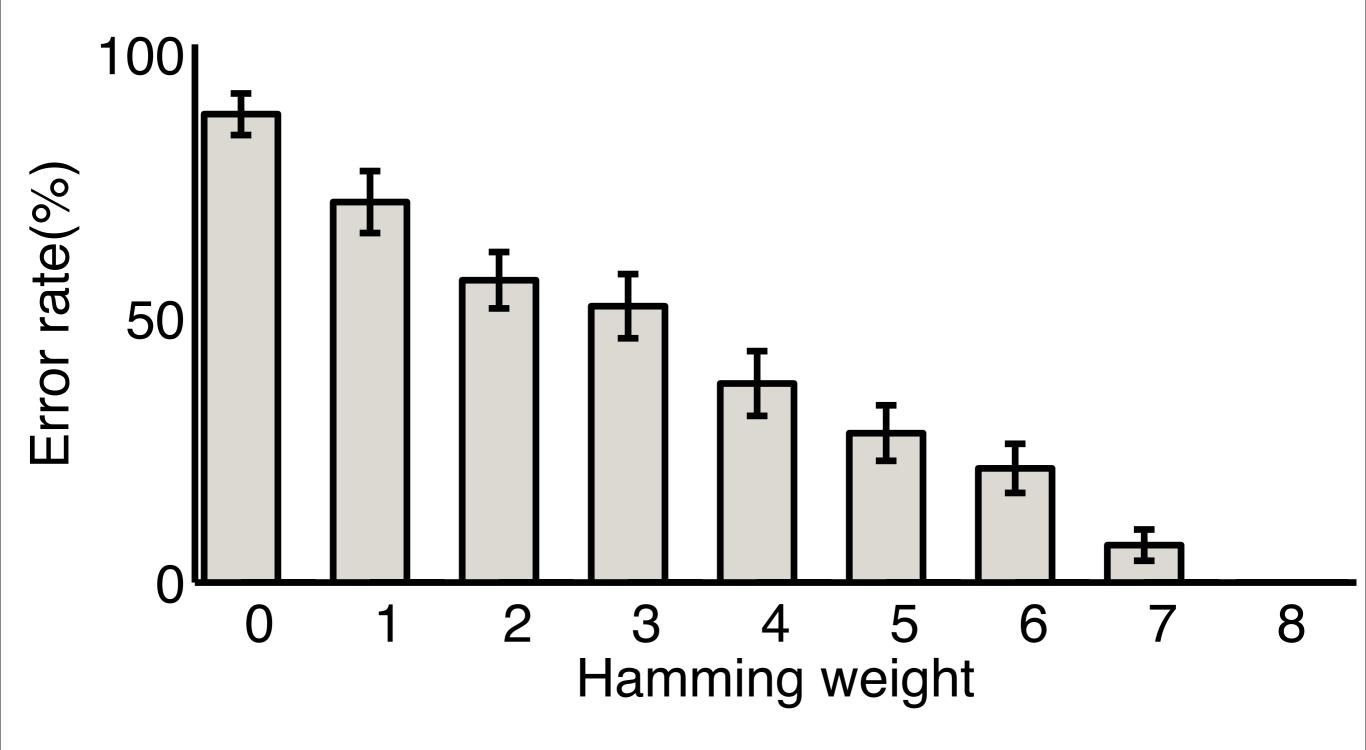




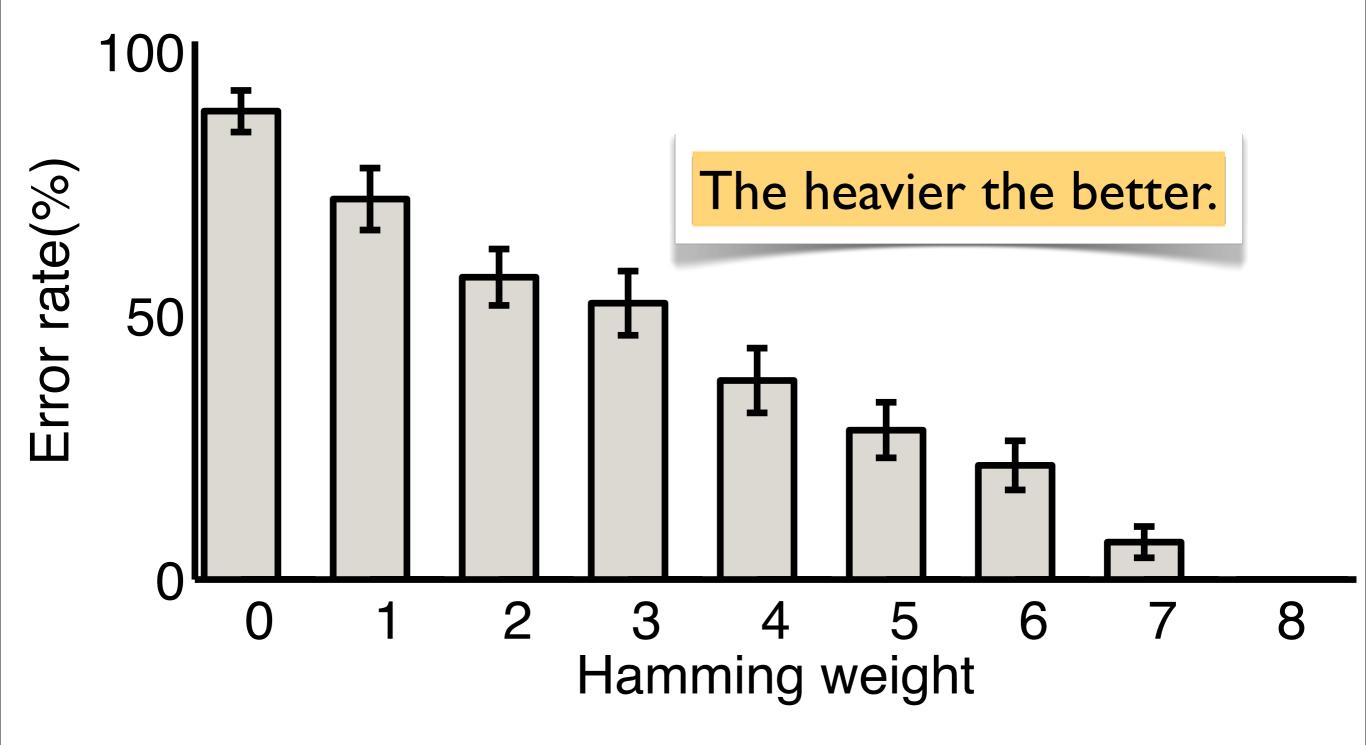


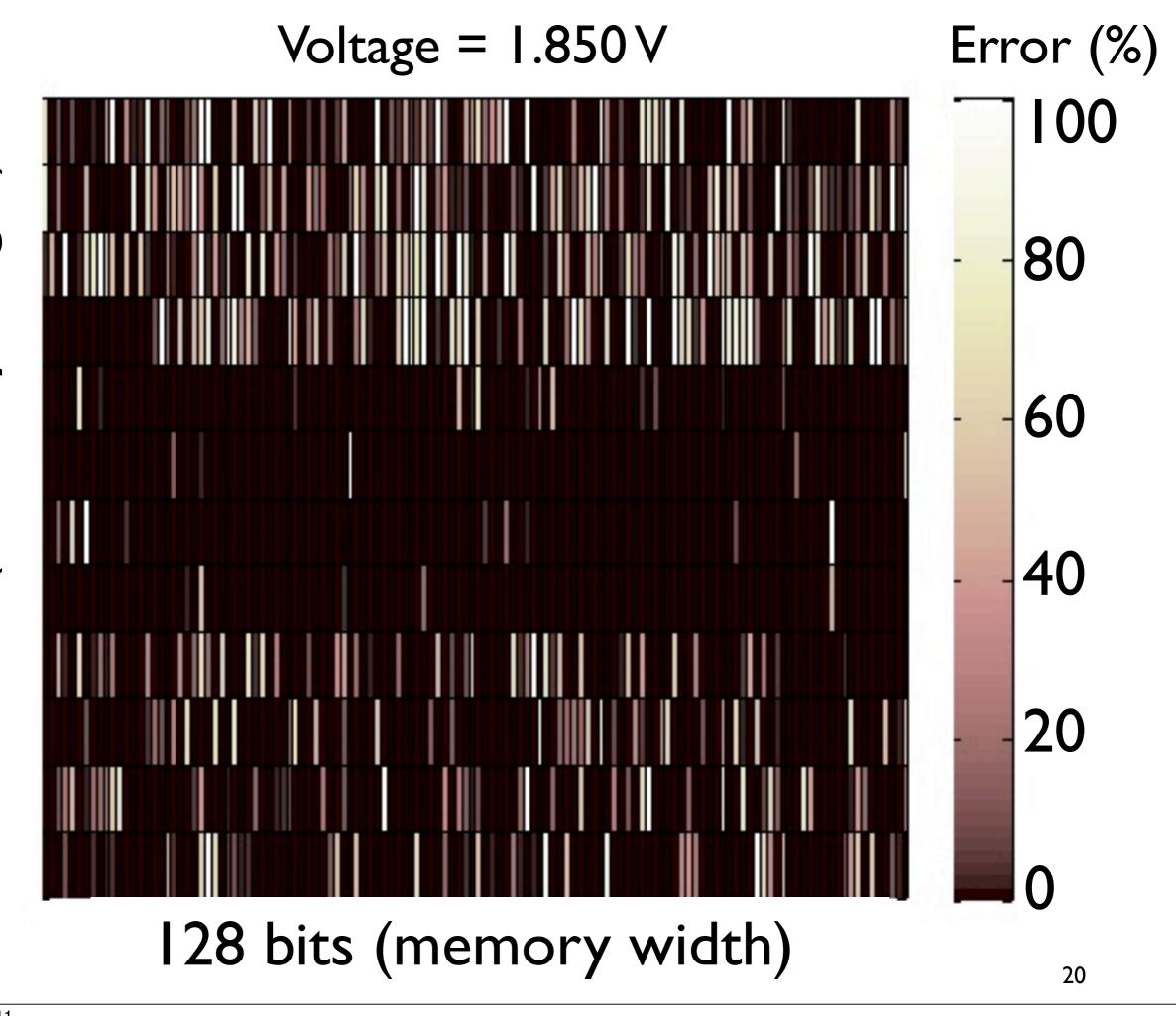


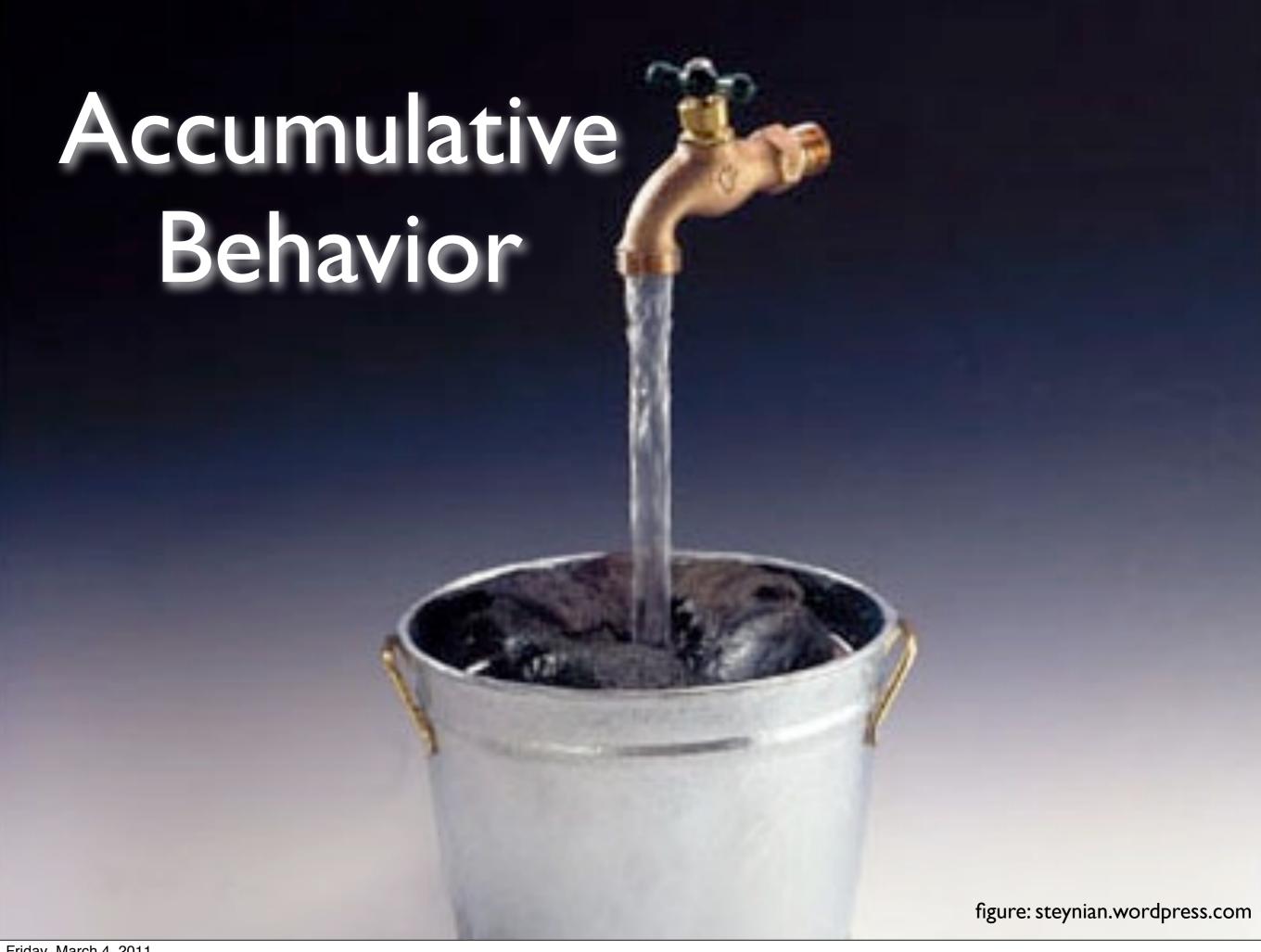
Data Hamming Weight



Data Hamming Weight







Design of a Low-voltage Storage

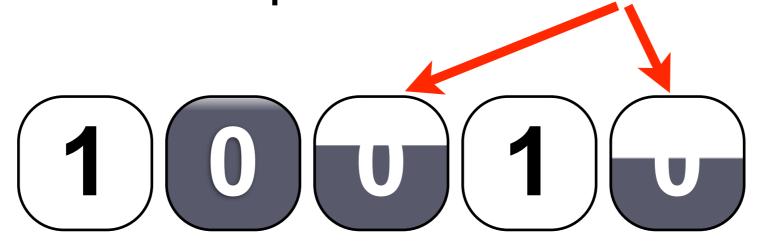
Modeling Flash Memory

- A set of n cells
- Cell state: $< c_1, ..., c_n >$
- $c_i \in \{0, 1\}$
- Initial state: $\forall i, c_i = 1$
- Update: set a subset of $\langle c_1, ..., c_n \rangle$ to 0
 - Once $c_i = 0$ then a write cannot $c_i \leftarrow 1$
 - Write Once Bits: Wits

Modeling Flash Memory

At low voltage:

- $c_i \leftarrow 0$ might fail and c_i remains 1. [Pavan:97]
- There might not be enough charge stored in a cell to represent a 0: Half-Wits



Design Goals

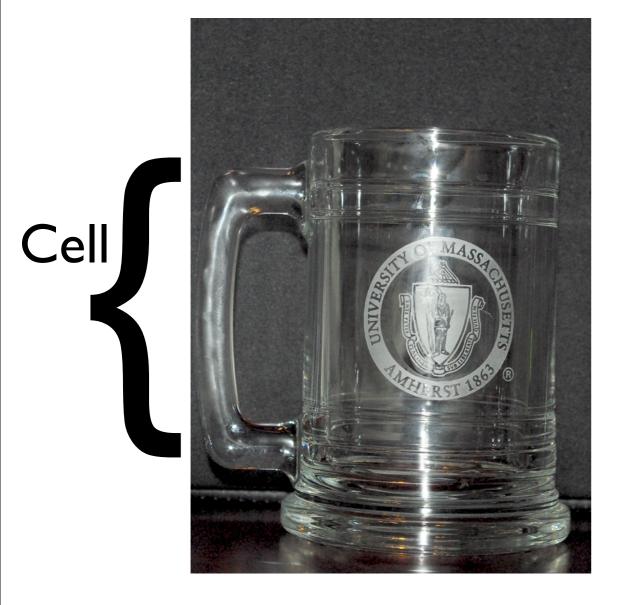
Minimize:

- Energy consumption
- Error rate
- Delay

Proposed Techniques

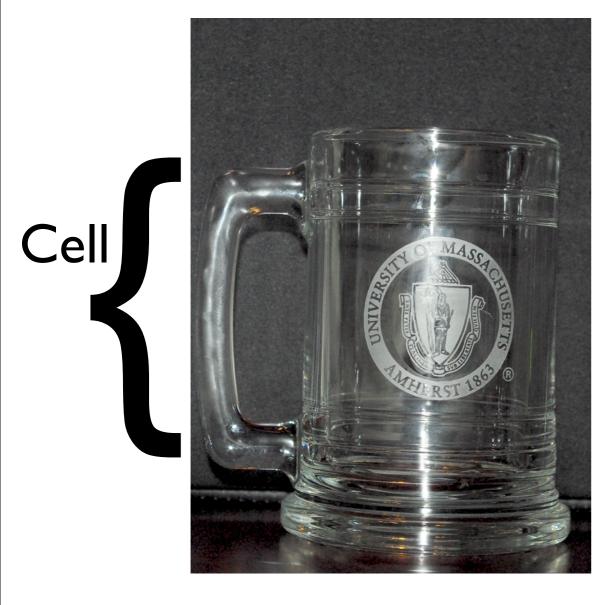
- I. In-place writes
- 2. Multiple-place writes
- 3. ReedSolomon-Berger Codes

Negative Logic



Initialization: I

Negative Logic



Initialization: I





Written: 0



Repeatedly attempt a write to the same location.

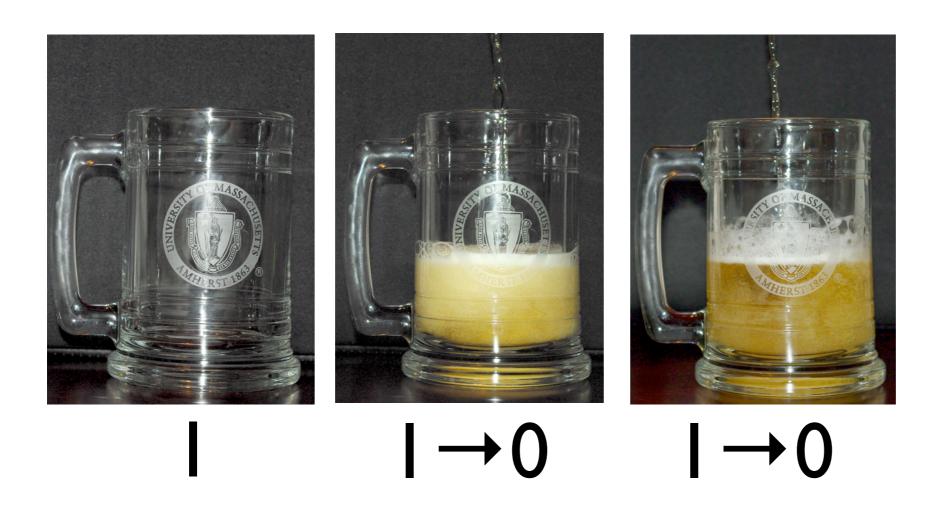
- Repeatedly attempt a write to the same location.
- Example: One bit over time



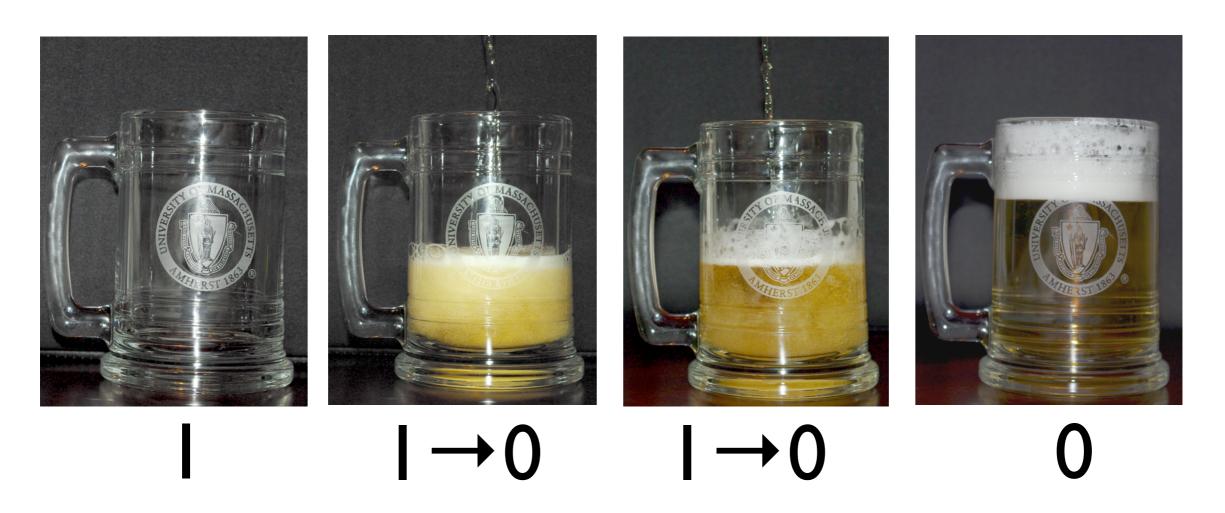
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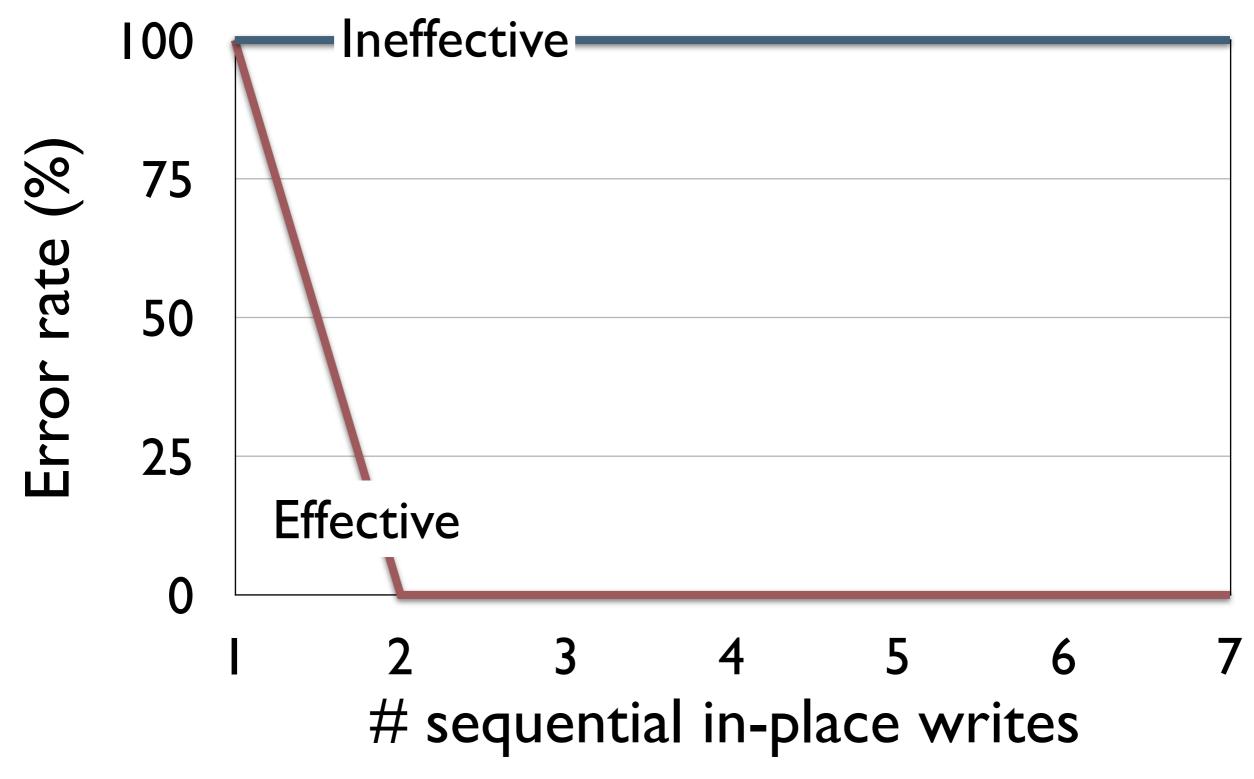


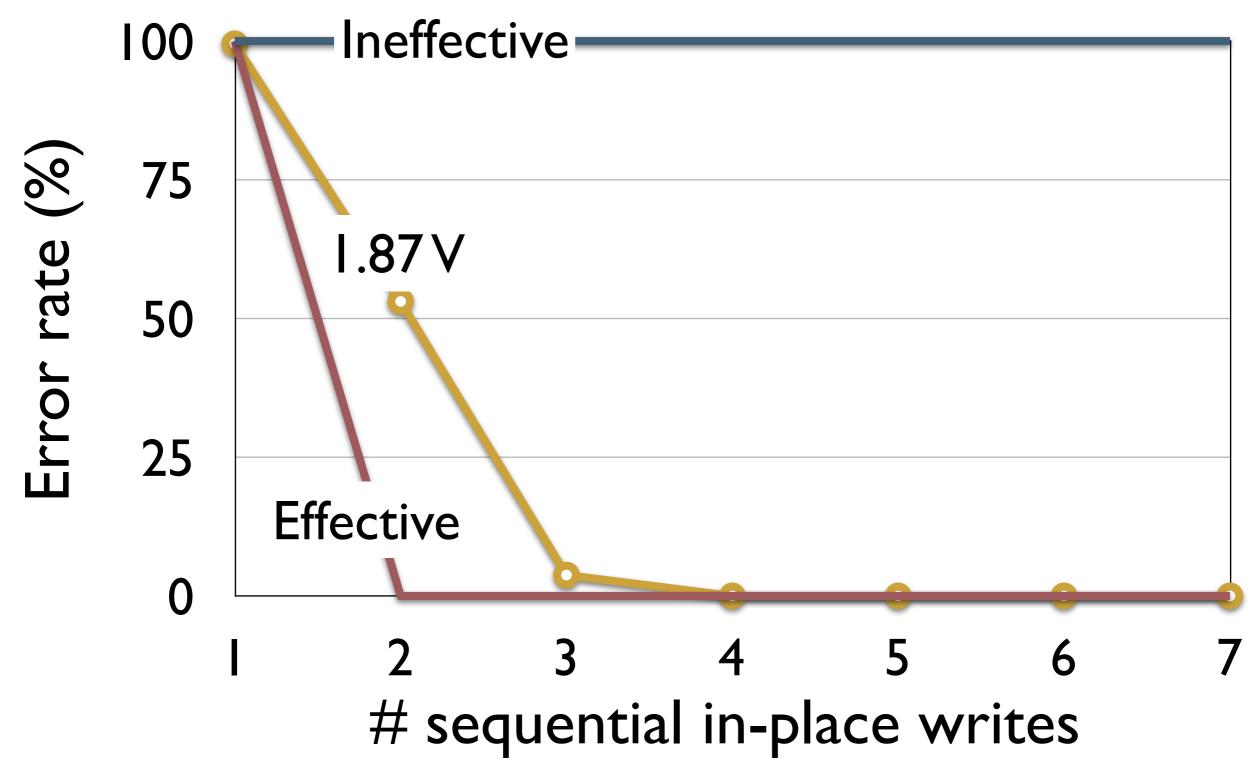
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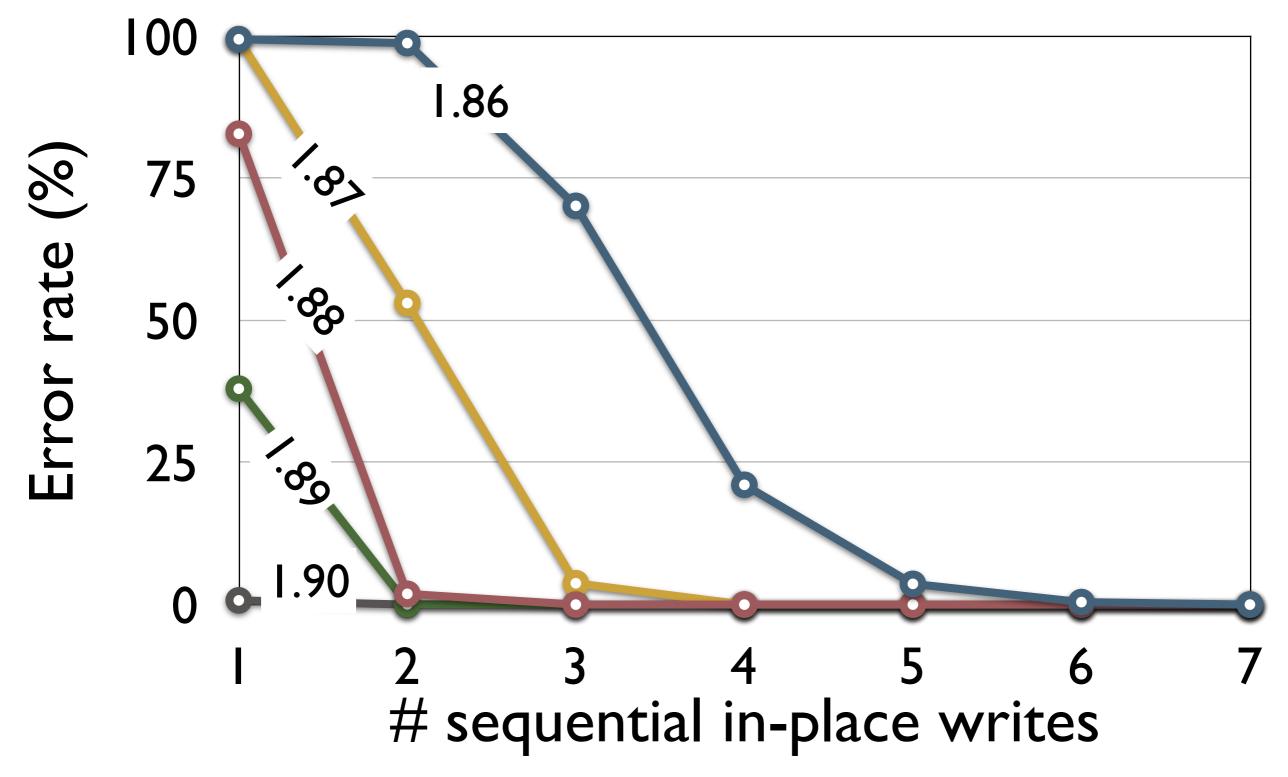


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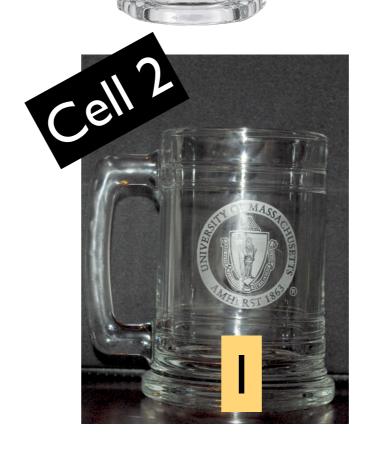








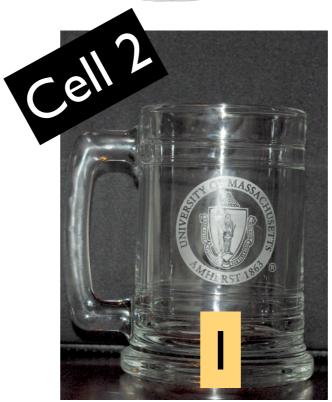
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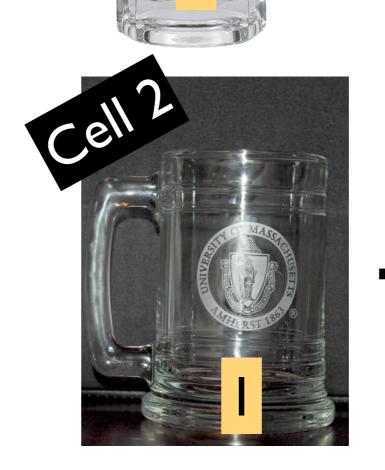






 Encoding: Write to more than one location.

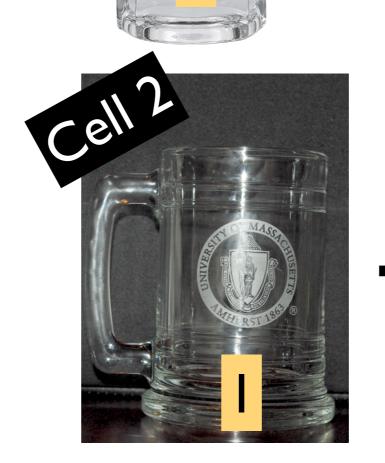
 Decoding: AND all of the values at read time.



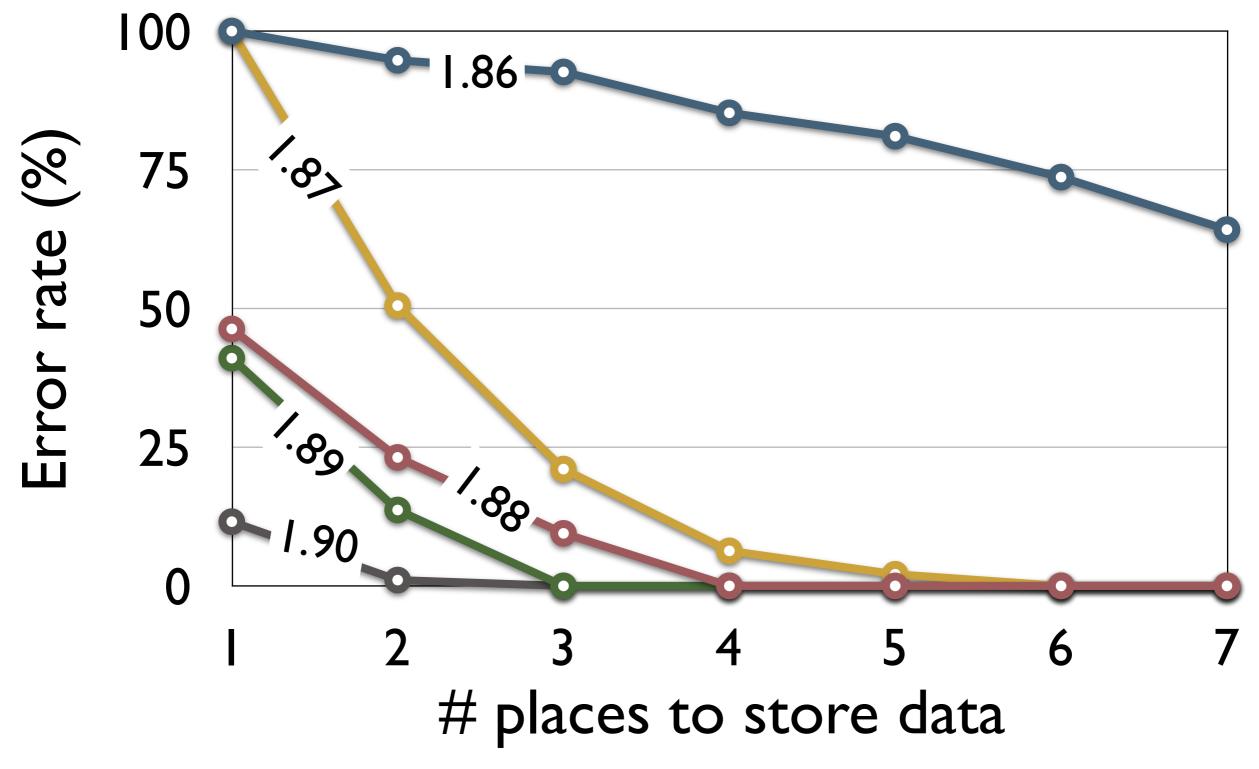


 Encoding: Write to more than one location.

 Decoding: AND all of the values at read time.







Design Goals

Minimize:

- Energy consumption
- Error rate



Delay

Comparison at 1.9 V

Store: Accelerometer trace
Repeating the writes 2 times/ locations

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Method	Time (ms)	Energy (µJ)
In-place	15.43	38
Multiple-place	16.85	40

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Micro-benchmarks:

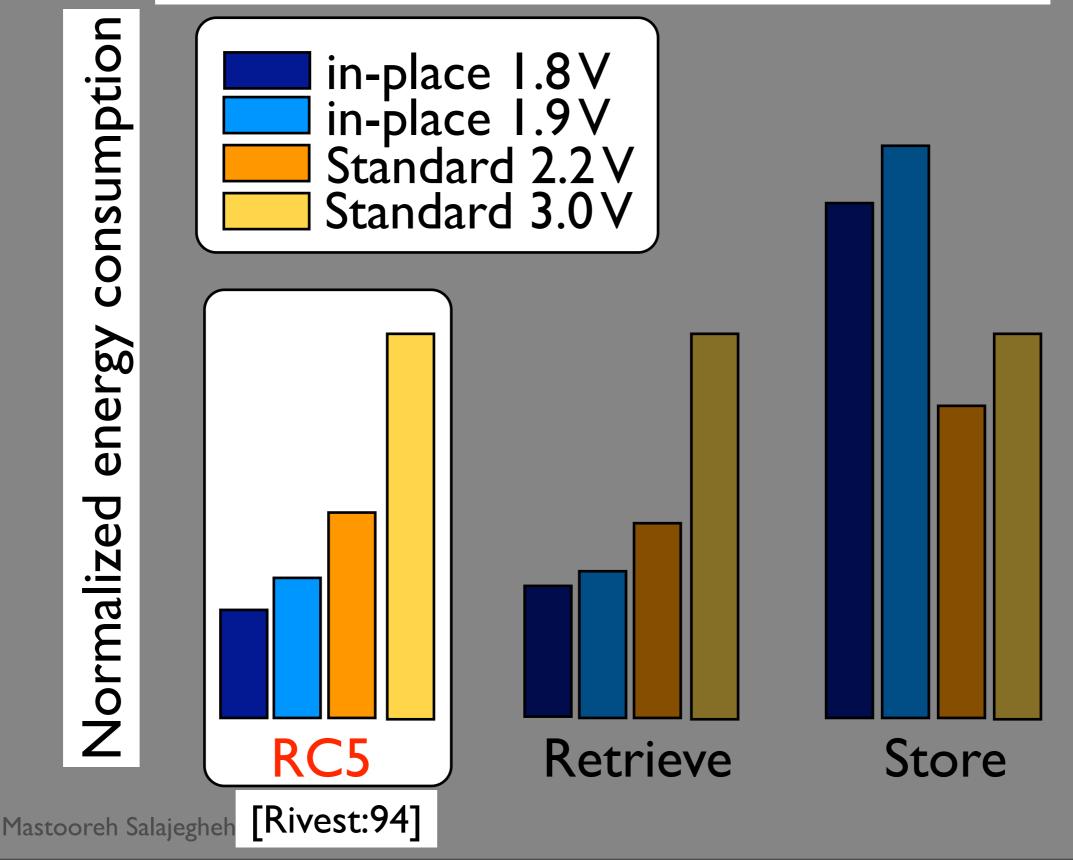
In-Place writes at low voltage

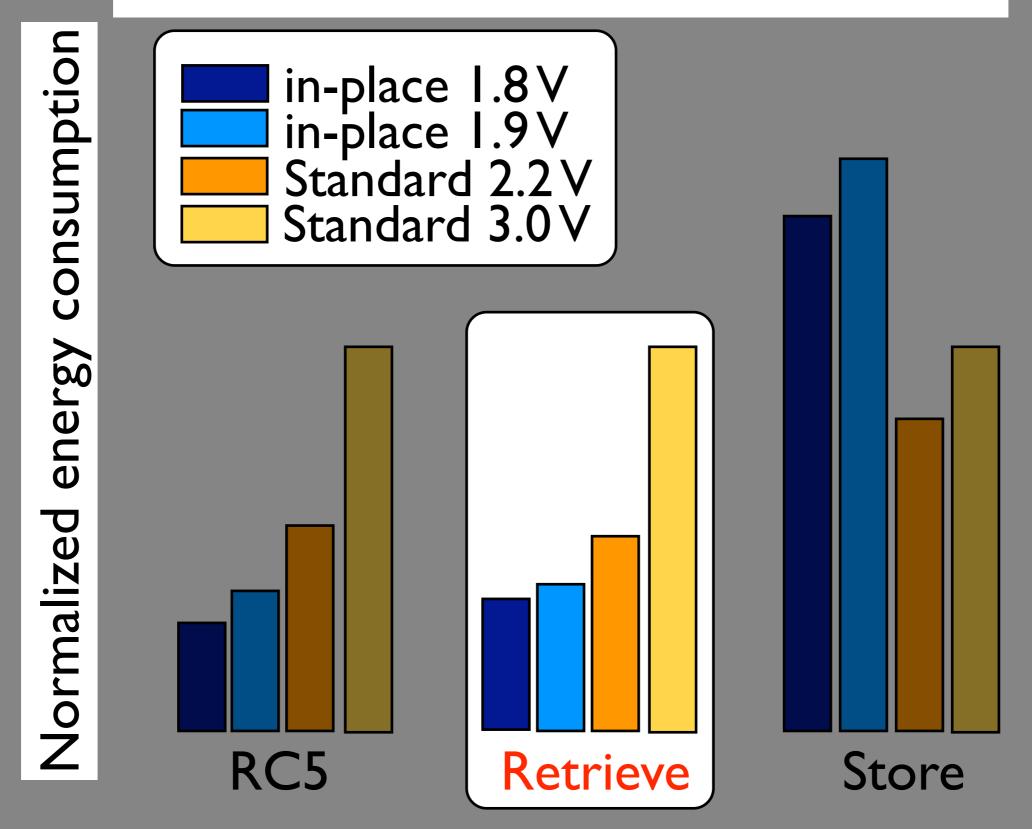
VS

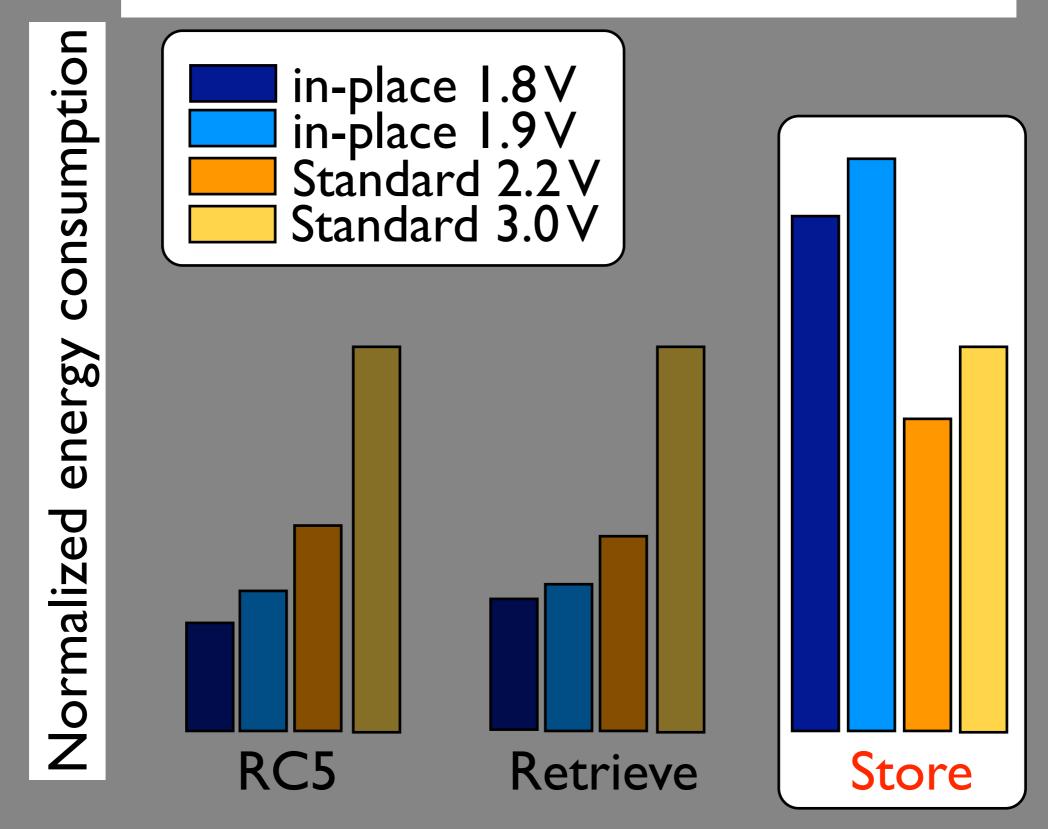
Standard approach

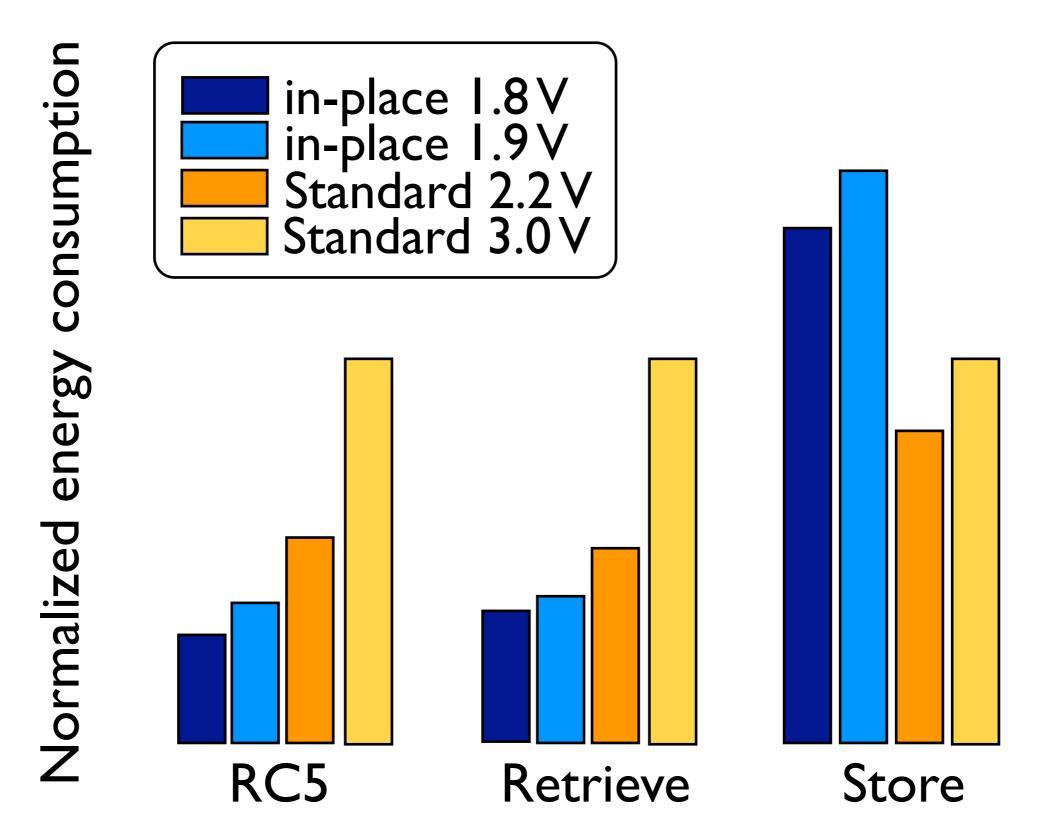
at

high voltage









Hypothesis

For CPU-bound workloads:

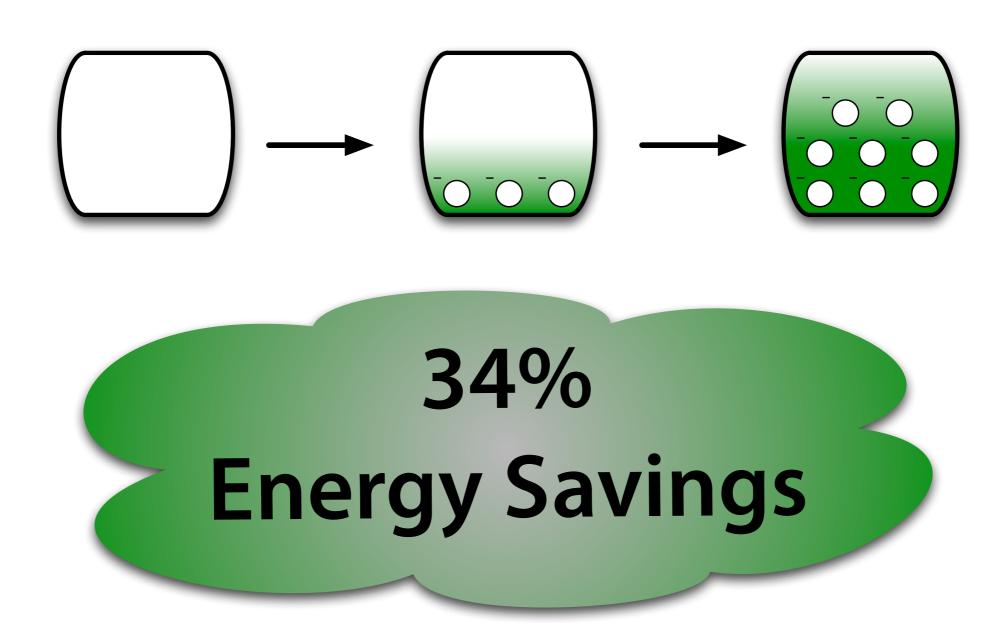
Energy of low-voltage system



Energy of high-voltage system

- Read 256 bytes of accelerometer data
- Aggregate data: Min, Max, Mean, Std. dev.
- Write the aggregation of 256 bytes of data

In-place Writes



Method	In-place	In-place	Standard	Standard
	1.8 v	1.9 V	2.2 V	3.0 V
Energy (µJ)	270	300	410	760

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Further improvements

I. Sign-bits and storing the complement [Papirla:09]

2. Memory mapping-table

Summary: Exploiting Half-Wits

- In-place writes on half-wits is an effective way to reduce wasted energy.
- Microcontrollers can work at a lower voltage and get more work done with the same amount of energy.
- The digital abstractions pay a higher price than necessary to provide reliability.

