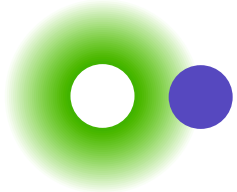
Dynamic Voltage and Frequency Scaling
The Laws of Diminishing Returns



Etienne Le Sueur and Gernot Heiser

HotPower'10, Vancouver, Canada, 2010
etienne.lesueur@nicta.com.au

What is DVFS?

Dynamic Voltage and Frequency Scaling

What is DVFS?

$$P = CfV^2$$

What is DVFS?

dynamic power consumption

$$P = CfV^2$$

What is DVFS?

dynamic power consumption

$$P = CfV^2$$

constant

What is DVFS?

dynamic power consumption

$$P = CfV^2$$

constant

frequency

What is DVFS?

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dynamic power consumption

voltage ***squared***

$$P = C f V^2$$

constant

frequency

In the past...

"Under some conditions, we observe energy savings of 30% for a 4% performance loss."

Snowdon et al. [2009]

In the past...

"... in most of the traces the potential for energy savings is good. The savings range from about 5% to about 75%, with most data points falling between 25% to 65% savings."

Weiser et al. [1994]

In the past...

"Energy savings of 22% ... to complete the same task are possible without a substantial reduction in application performance..."

Weissel et al. [2002]

In the past...

"... Hence, on this system, by lowering the frequency to a point where the workloads can be adequately served without sacrificing latency, energy is saved."

Miyoshi et al. [2002]

The whole story

$$P = CfV^2 + P_{static}$$

The whole story

total power consumption

$$P = CfV^2 + P_{static}$$

The whole story

total power consumption

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dynamic power consumption

The whole story

total power consumption

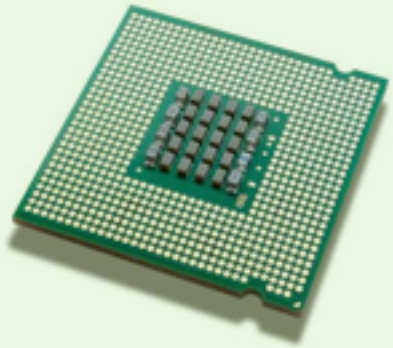
static power consumption

$$P = CfV^2 + P_{static}$$

dynamic power consumption

Static power consumption

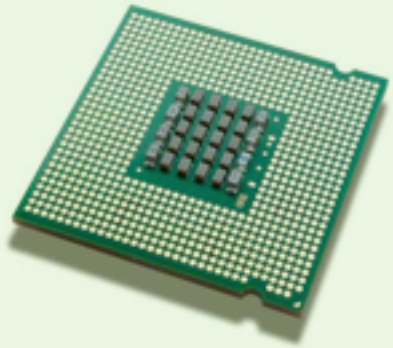
Static power consumption



CPU leakage

Static power consumption

Hard drives



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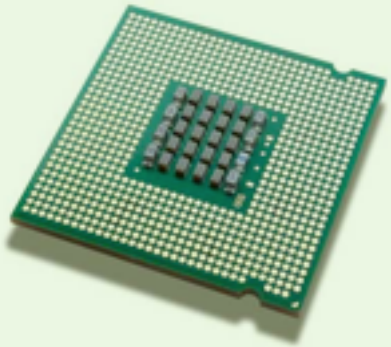
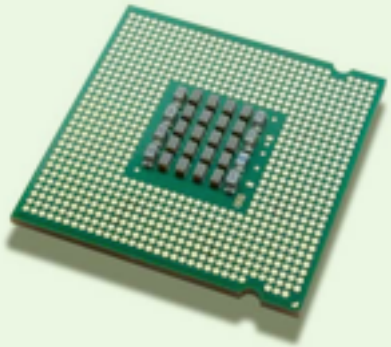


CPU leakage

Memory

Static power consumption

Hard drives



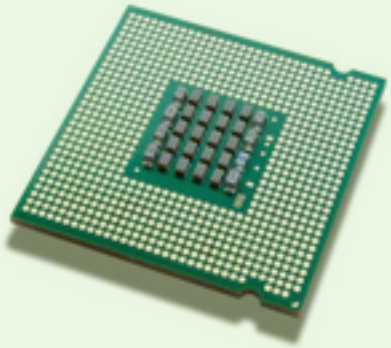
CPU leakage

Memory

Power supply losses

Static power consumption

Hard drives



CPU leakage

Memory

Power supply losses

etc.

How can DVFS save energy?

```
400c30:       48 8b 11              mov    (%rcx),%rdx
400c33:       48 8b 42 48           mov    0x48(%rdx),%rax
400c37:       48 89 41 10           mov    %rax,0x10(%rcx)
400c3b:       48 89 4a 48           mov    %rcx,0x48(%rdx)
400c3f:       48 8b 51 08           mov    0x8(%rcx),%rdx
400c43:       48 8b 42 50           mov    0x50(%rdx),%rax
400c47:       48 89 41 18           mov    %rax,0x18(%rcx)
400c4b:       48 89 4a 50           mov    %rcx,0x50(%rdx)
400c4f:       48 83 c1 40           add    $0x40,%rcx
```

[SPEC CPU2000, 181.mcf, gcc 4.2, high optimisation]

How can DVFS save energy?

```
400c30:       48 8b 11              mov    (%rcx),%rdx
400c33:       48 8b 42 48           mov    0x48(%rdx),%rax
400c37:       48 89 41 10           mov    %rax,0x10(%rcx)
400c3b:       48 89 4a 48           mov    %rcx,0x48(%rdx)
400c3f:       48 8b 51 08           mov    0x8(%rcx),%rdx
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[SPEC CPU2000, 181.mcf, gcc 4.2, high optimisation]

... such workloads can be ***memory-bound***

How can DVFS save energy?

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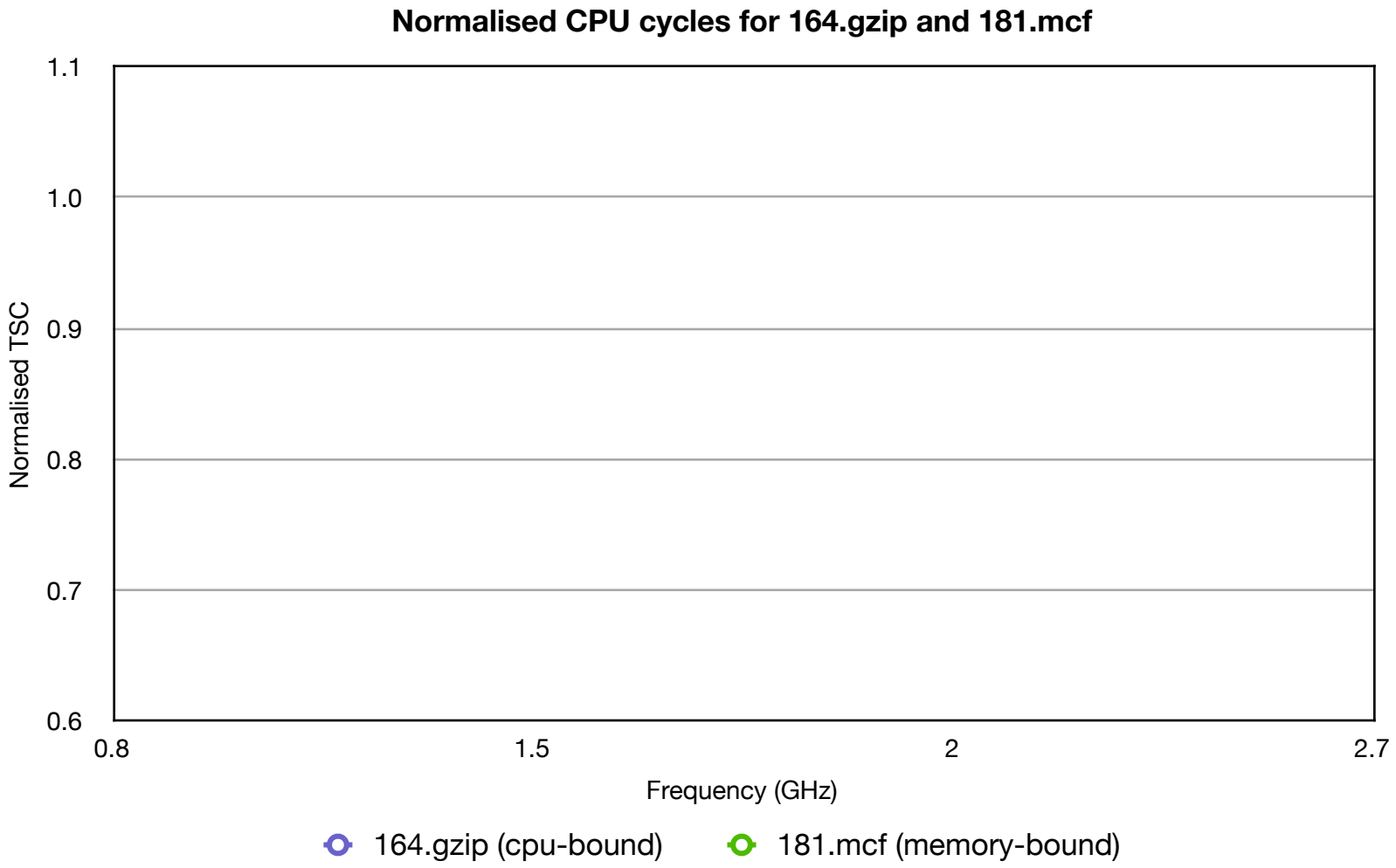

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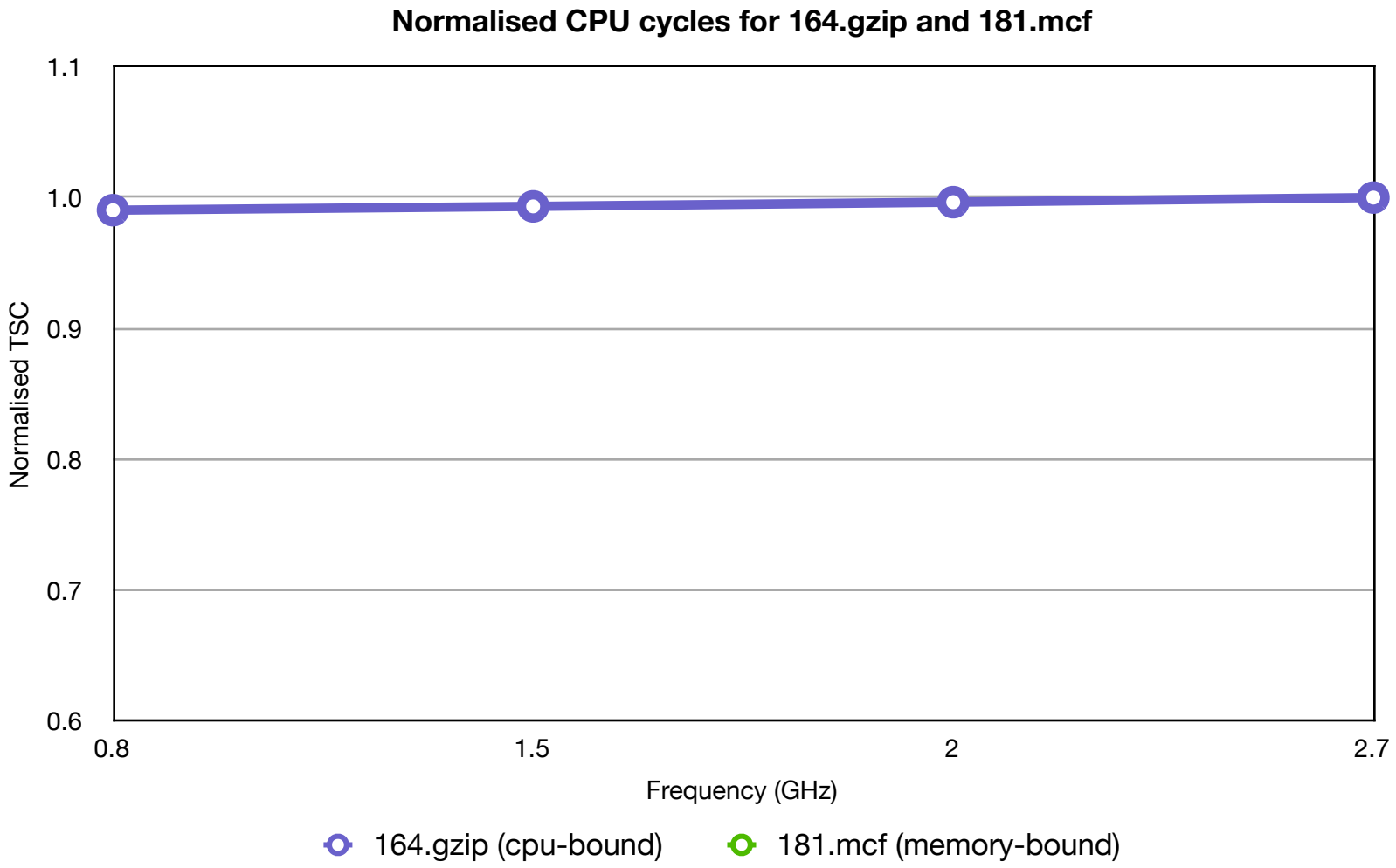

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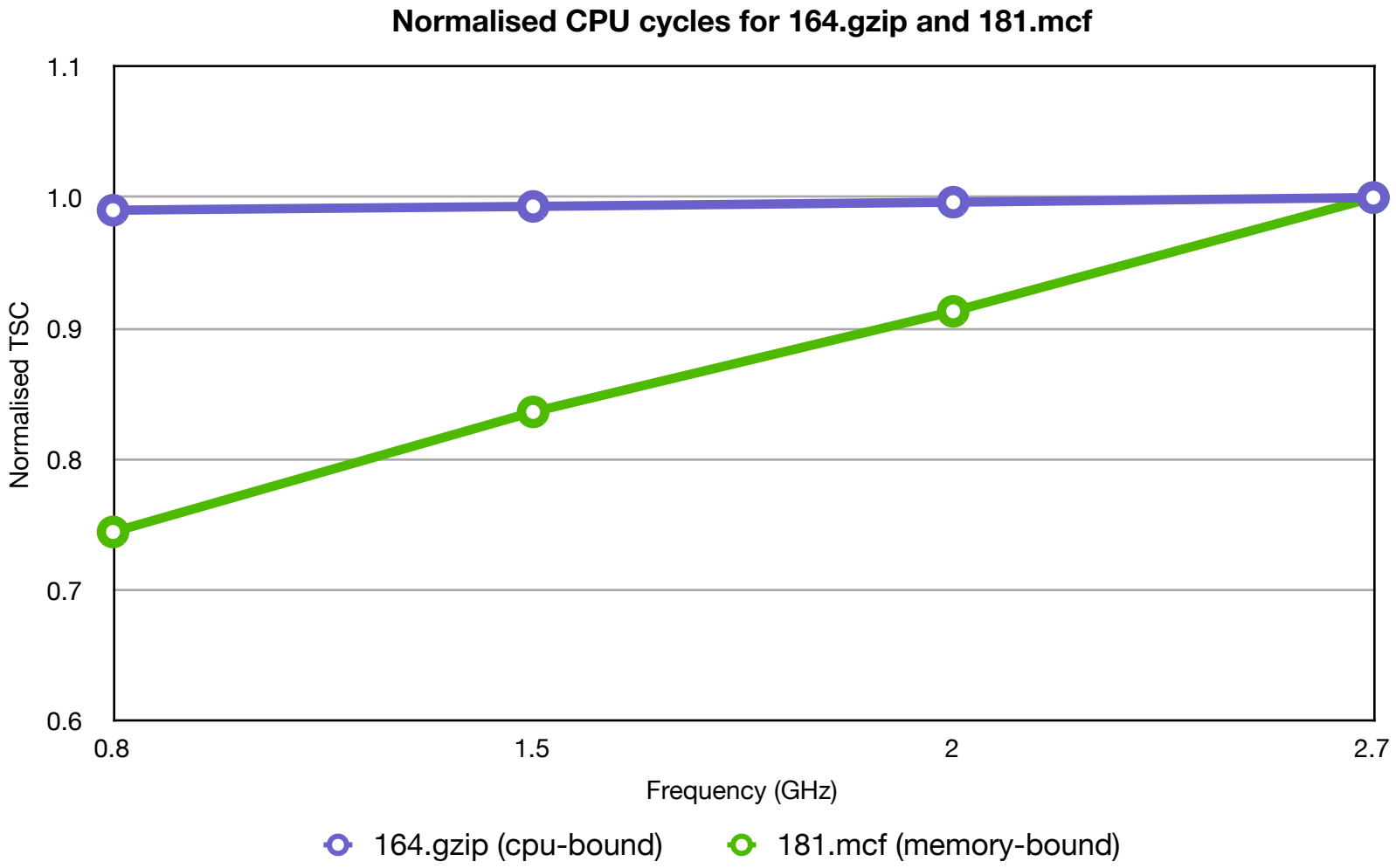

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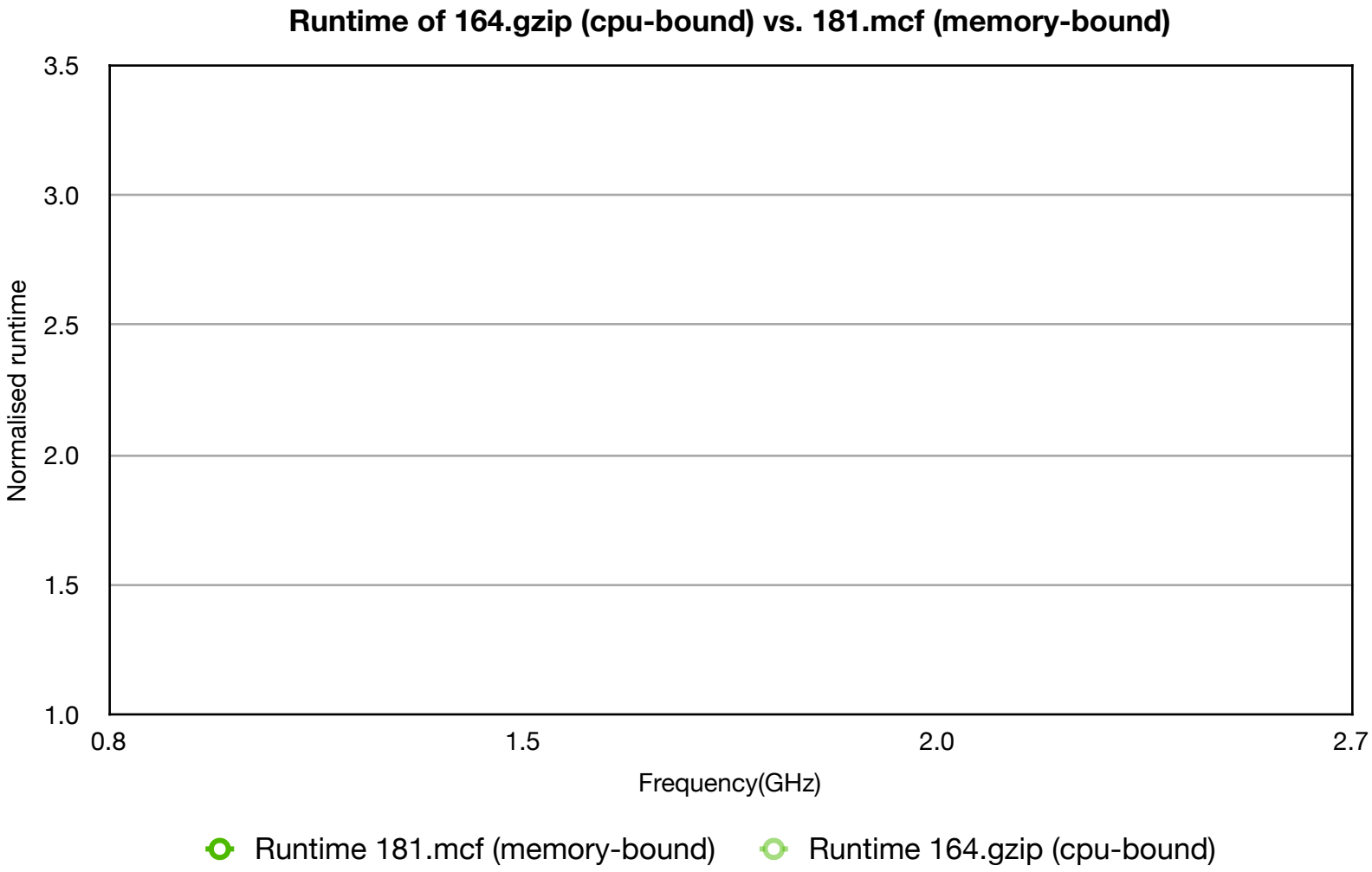

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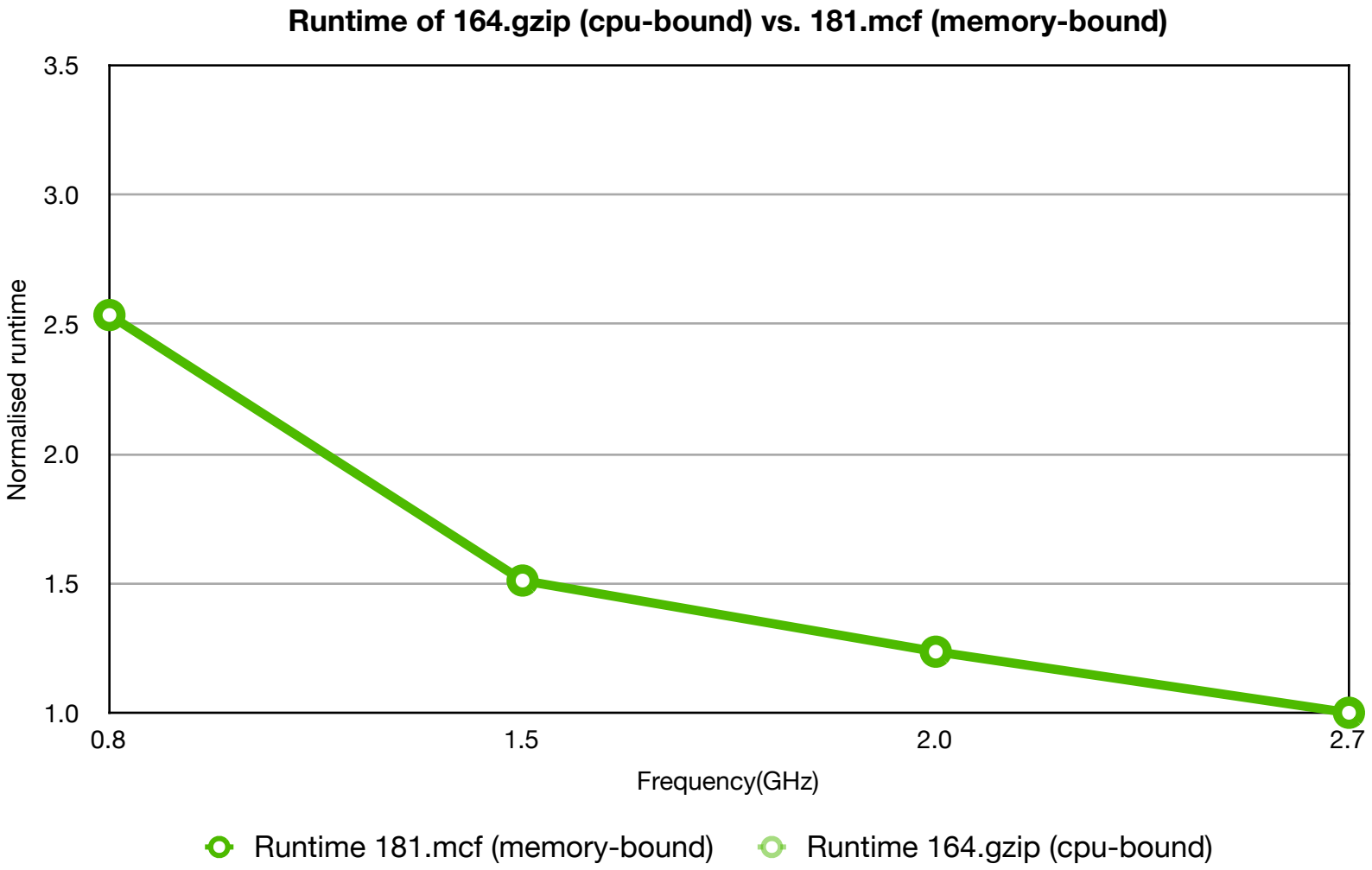

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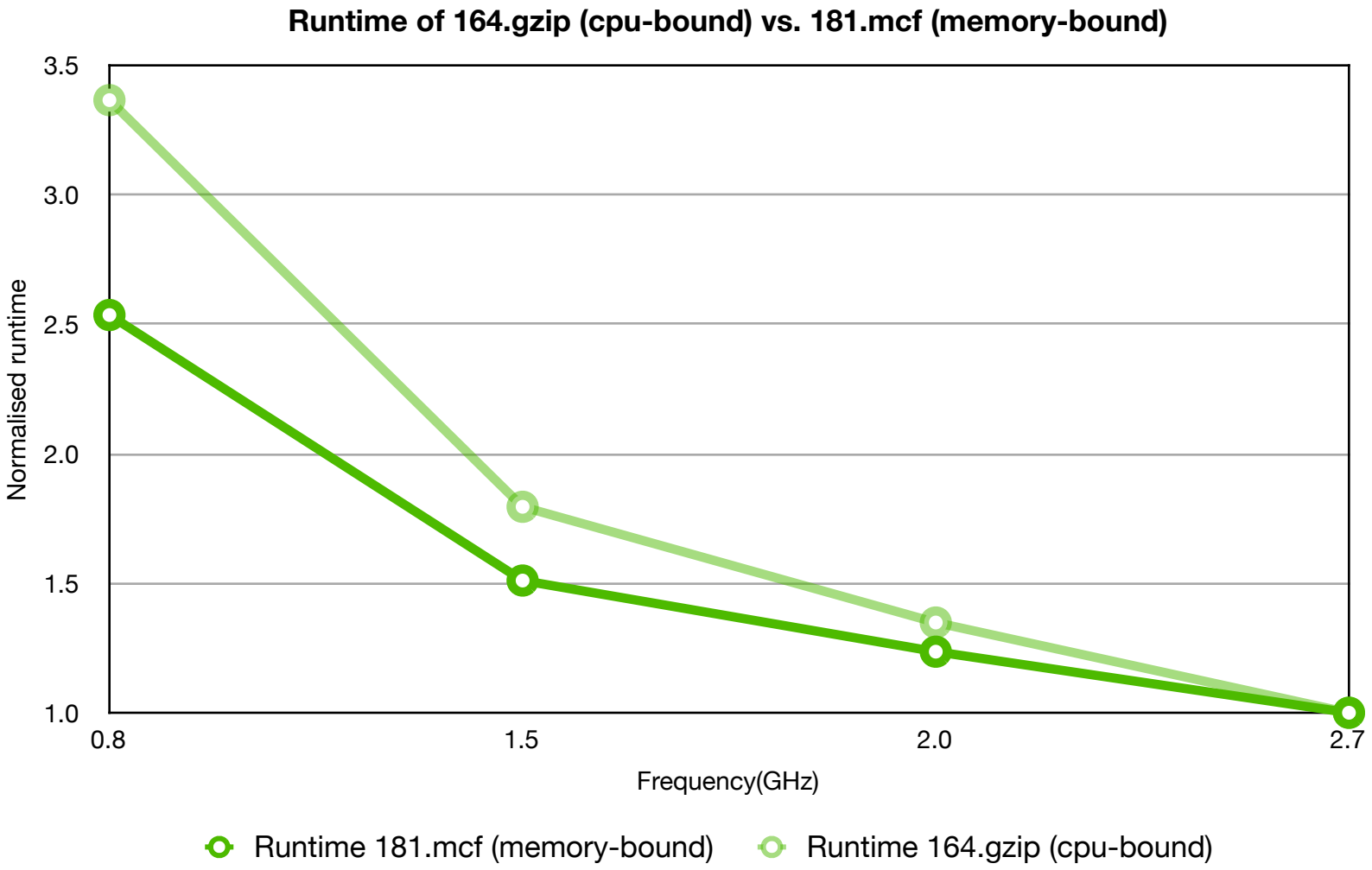


Our analysis

NICTA

3 generations of ***AMD Opteron*** CPUs
in server-class systems

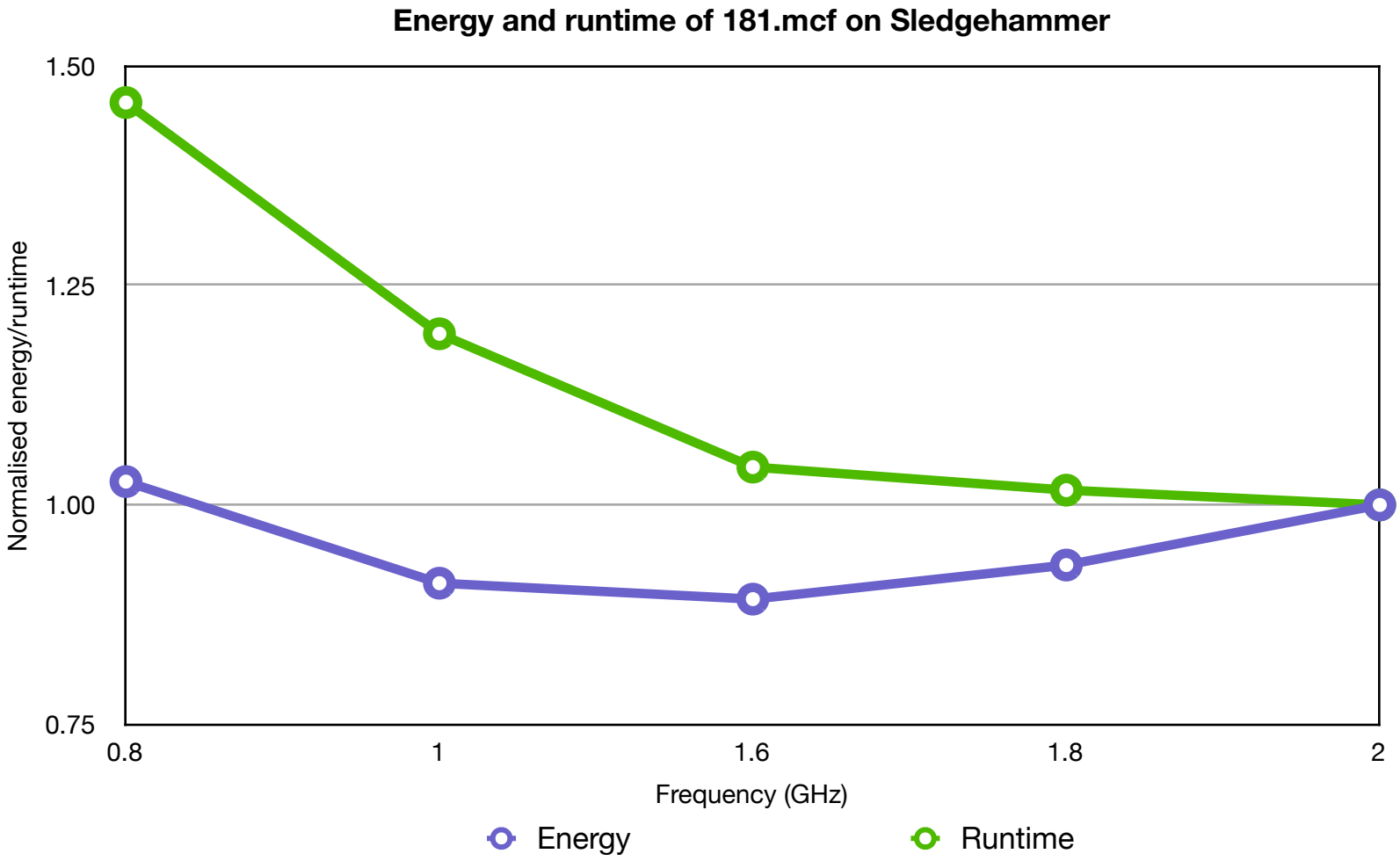
Our analysis

Die codename	Sledgehammer		
Year	2003		
Core count	1		
Frequency range	0.8 - 2.0GHz		
Voltage range	0.9 - 1.5		
Process	130nm		
TDP	89W		
Die area	193mm^2		
Transistor count	106M		

Sledgehammer

NICTA

Sledgehammer

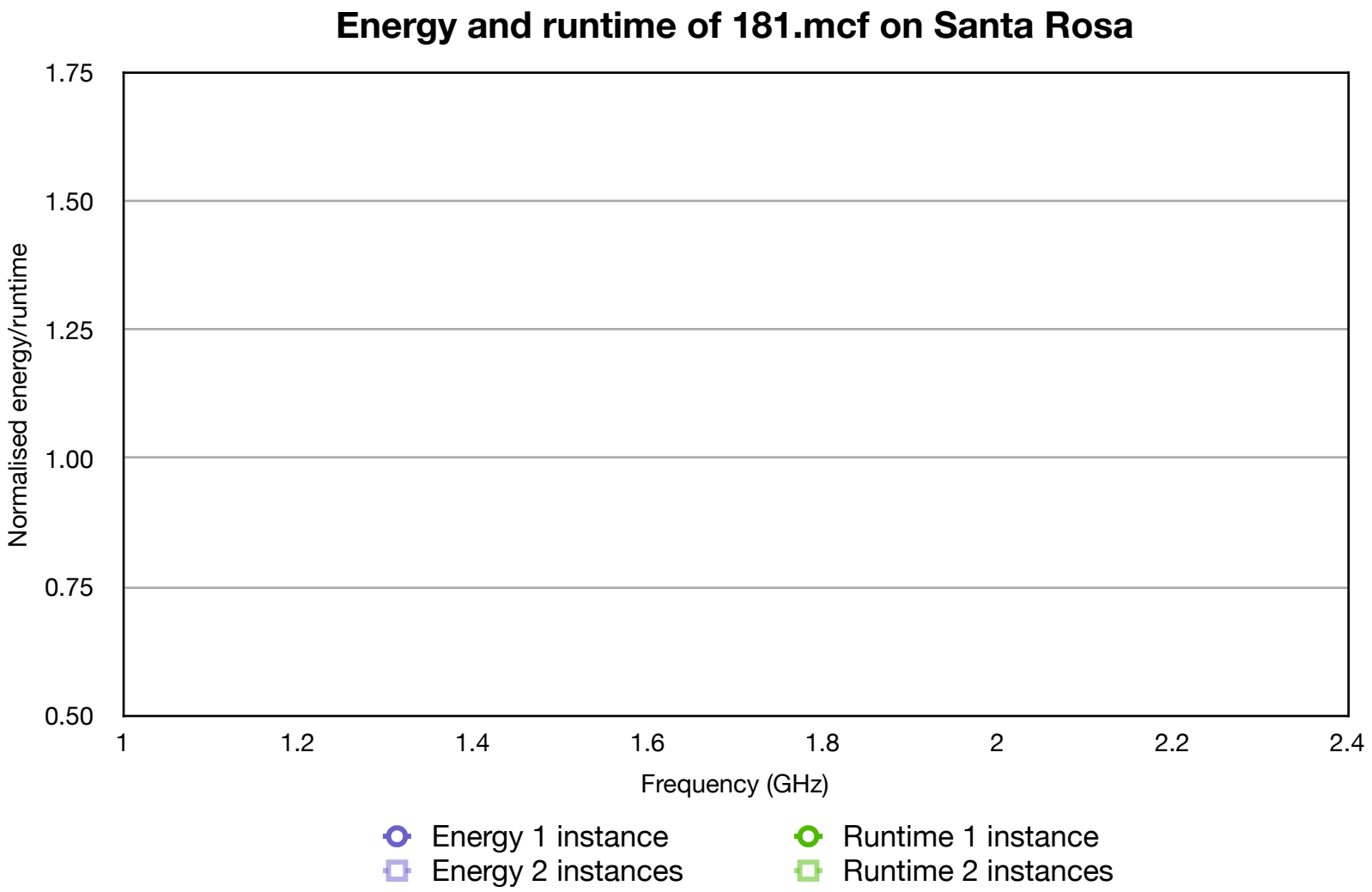


Our analysis

Die codename	Sledgehammer	**Santa Rosa**
Year	2003	**2006**
Core count	1	**2**
Frequency range	0.8 - 2.0GHz	**1.0 - 2.4GHz**
Voltage range	0.9 - 1.5	**0.9 - 1.35V**
Process	130nm	**90nm**
TDP	89W	**95W**
Die area	193mm^2	**230mm^2**
Transistor count	106M	**243M**

Santa Rosa

Santa Rosa



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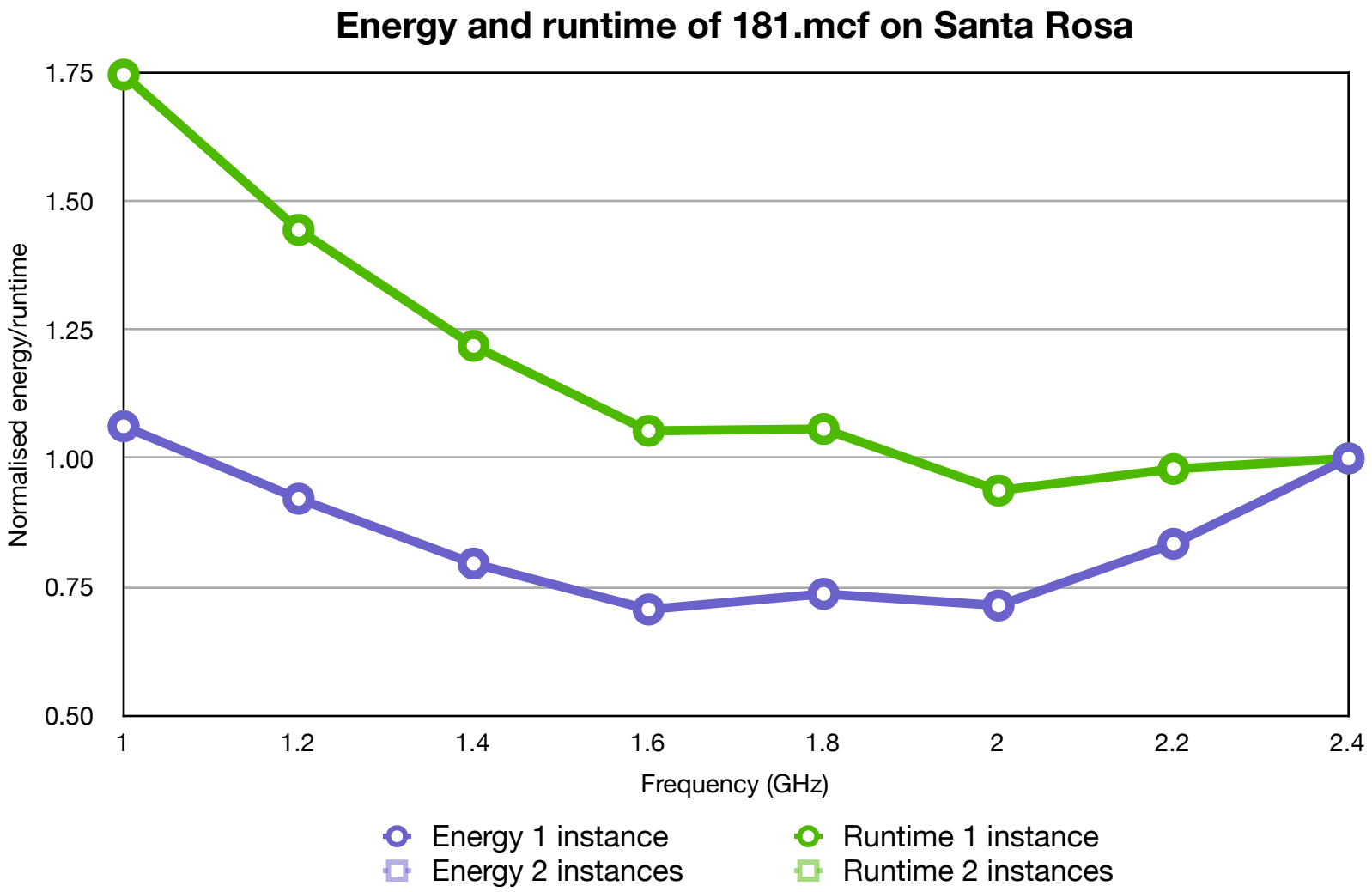
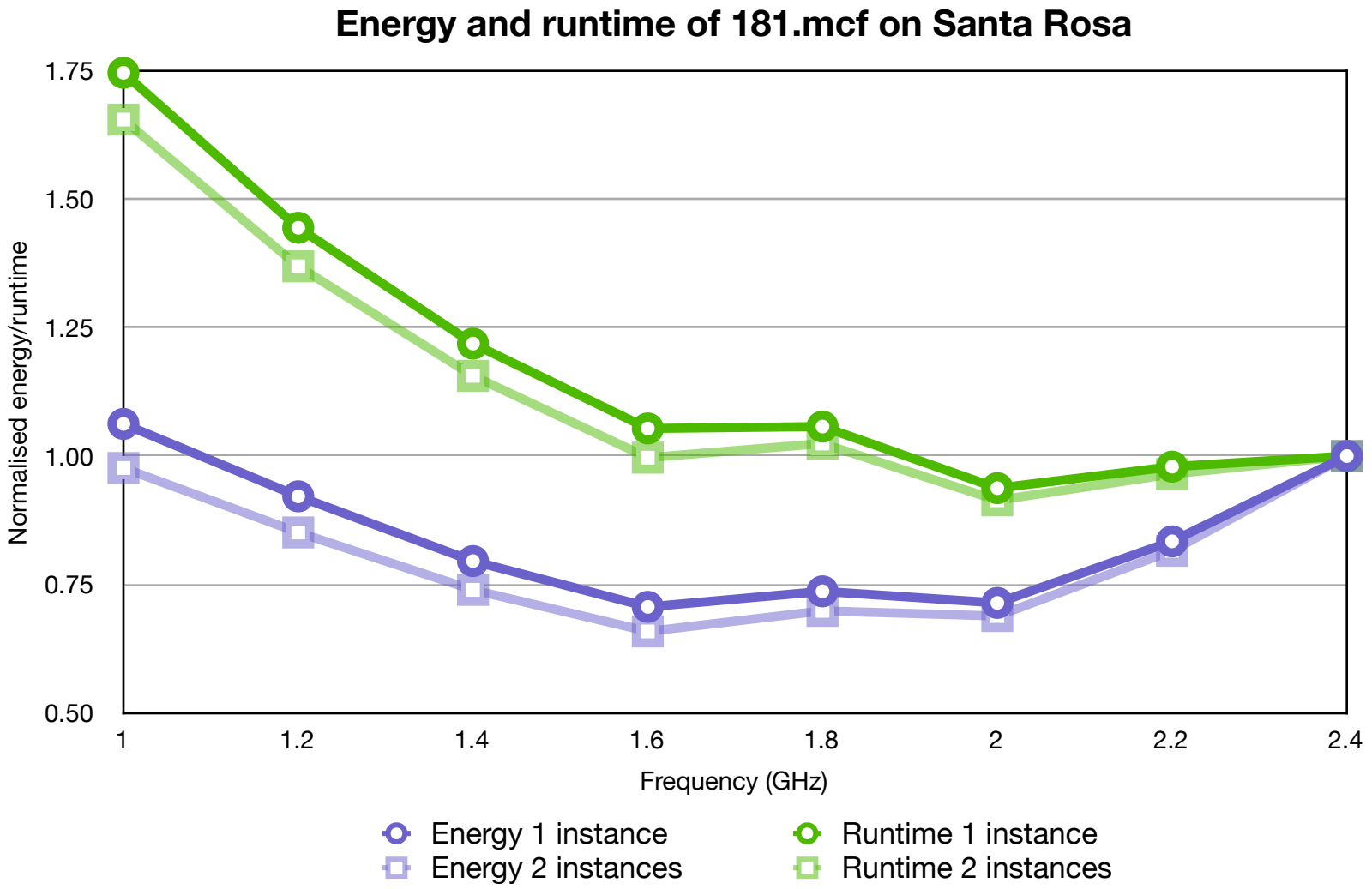


Santa Rosa



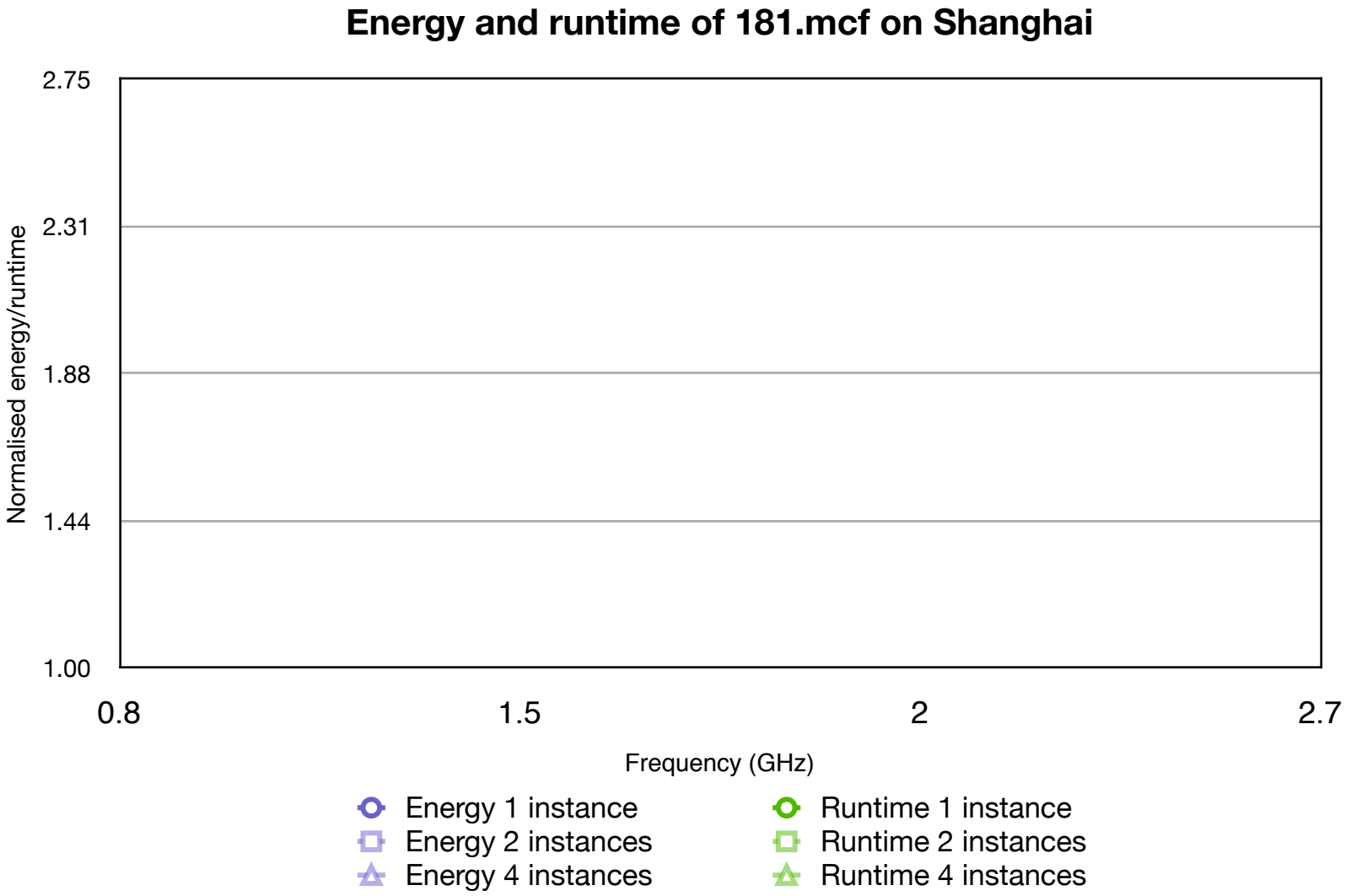
Our analysis

Die codename	Sledgehammer	Santa Rosa	**Shanghai**
Year	2003	2006	**2009**
Core count	1	2	**4**
Frequency range	0.8 - 2.0GHz	1.0 - 2.4GHz	**0.8 - 2.7GHz**
Voltage range	0.9 - 1.5	0.9 - 1.35V	**1.0 - 1.35V**
Process	130nm	90nm	**45nm**
TDP	89W	95W	**75W**
Die area	193mm^2	230mm^2	**285mm^2**
Transistor count	106M	243M	**463M**

Shanghai

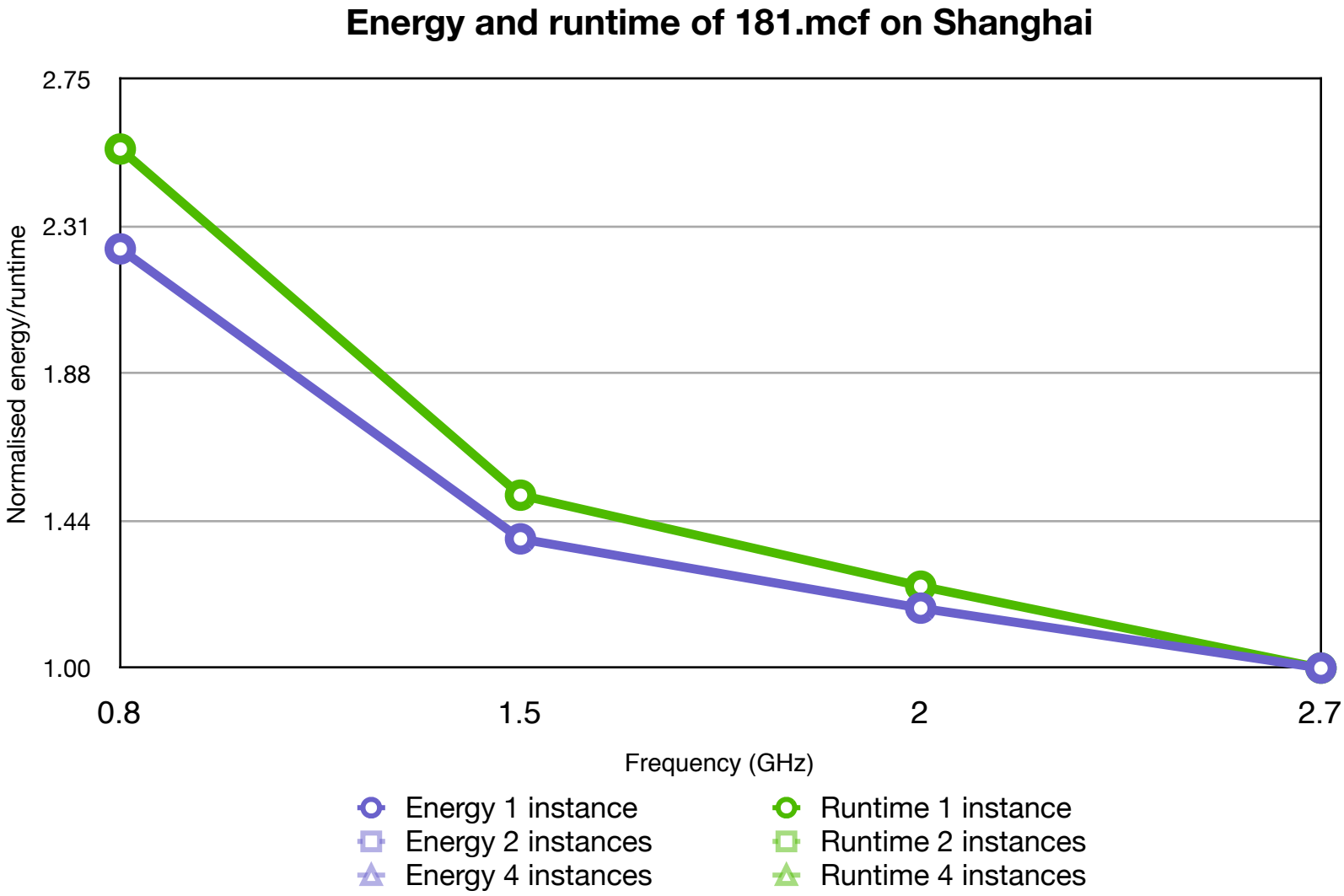
Shanghai

NICTA



Shanghai

NICTA



Shanghai

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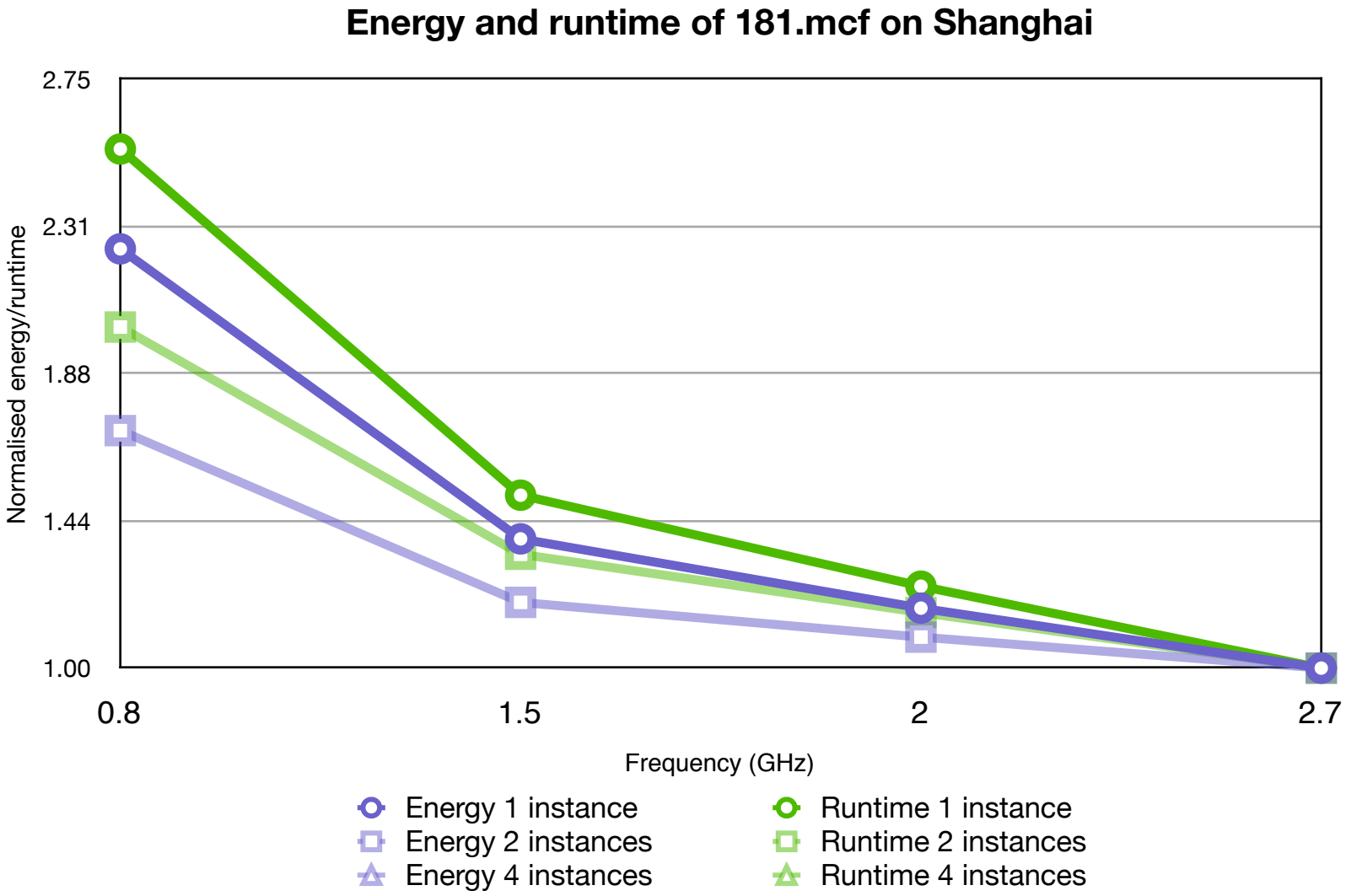
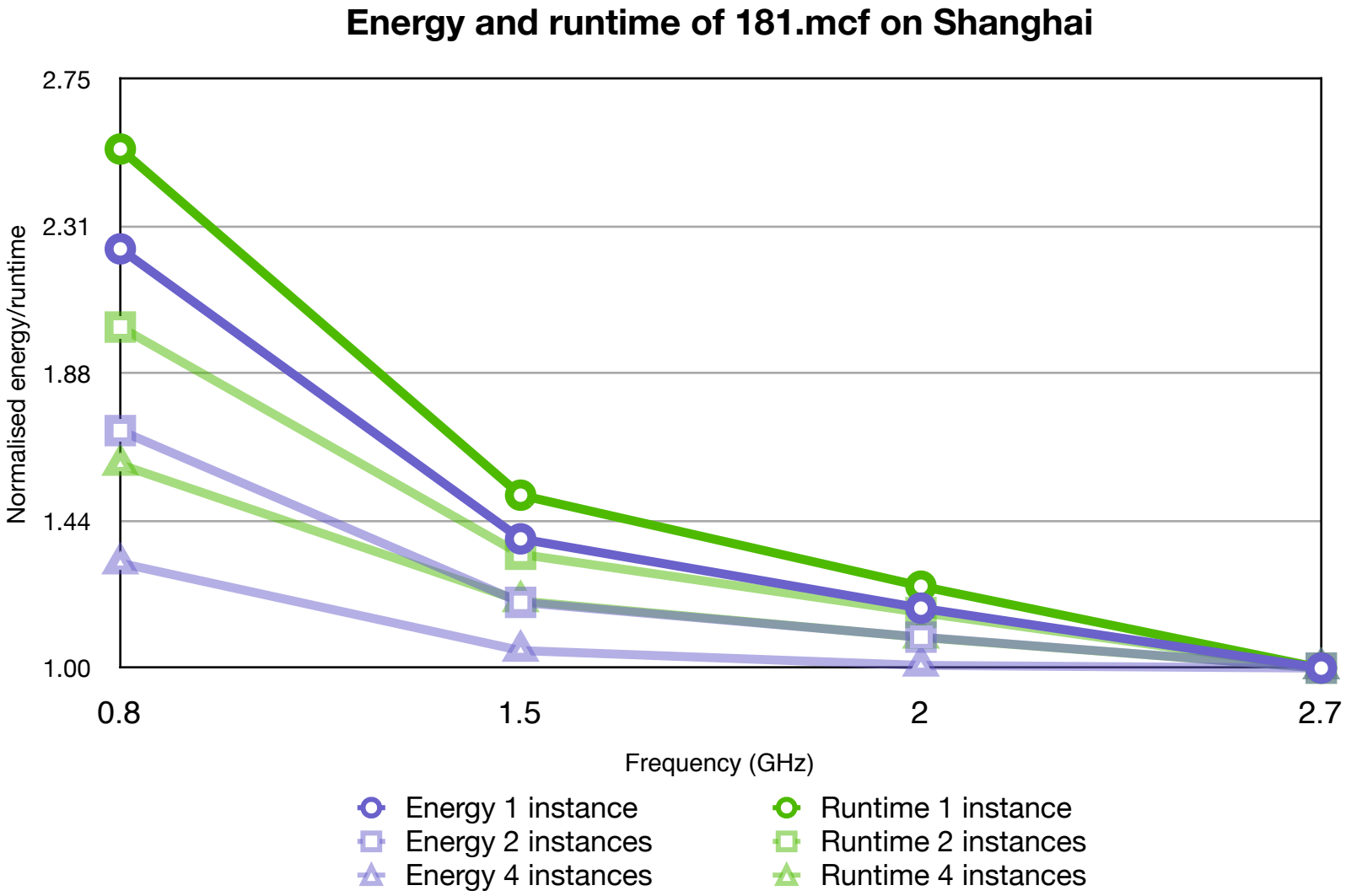


Shanghai

NICTA



Results

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DVFS on Shanghai is ***ineffective for saving energy!***

Results

NICTA

DVFS on Shanghai is ***ineffective for saving energy!***

... but ***why?***

Static power

DVFS can only change ***dynamic*** power consumption and static power is increasing!

What are the trends?

What are the trends?

- scaling of transistor technology;

What are the trends?

- scaling of transistor technology;
- increasing memory performance;

What are the trends?

- scaling of transistor technology;
- increasing memory performance;
- improved idle/sleep modes; and

What are the trends?

- scaling of transistor technology;
- increasing memory performance;
- improved idle/sleep modes; and
- multi-core processors.

Scaling of transistor technology

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In ~7 years:

Scaling of transistor technology

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In ~7 years:

- 130 nm to 45 nm

Scaling of transistor technology

NICTA

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Scaling of transistor technology

NICTA

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- 193 mm^2 to 285 mm^2

Scaling of transistor technology

NICTA

In ~7 years:

- 130 nm to 45 nm
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- 193 mm^2 to 285 mm^2
- 1 MiB to 8 MiB total SRAM cache

Scaling of transistor technology

NICTA

In ~7 years:

- 130 nm to 45 nm
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- 1 MiB to 8 MiB total SRAM cache
- Single to quad-core (more later...)

Scaling of transistor technology

NICTA

In ~7 years:

- 130 nm to 45 nm
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- 193 mm^2 to 285 mm^2
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- Single to quad-core (more later...)

Static power is increasing significantly, dynamic power is decreasing

Increasing memory performance

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In ~7 years:

Increasing memory performance

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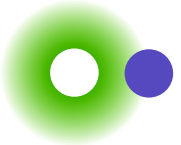
In ~7 years:

- Much larger CPU SRAM caches (fewer cache-misses)



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Increasing memory performance

NICTA

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Fewer pipeline stalls for memory references means code is less memory-bound

Improved idle/sleep modes

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In ~7 years:

Improved idle/sleep modes

NICTA

In ~7 years:

- From a single ‘halt’ mode (ACPI C1)

Improved idle/sleep modes

NICTA

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Improved idle/sleep modes

NICTA

In ~7 years:

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Push towards race-and-halt

Multi-core processors

Today:

Multi-core processors

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Today:

- Single off-chip voltage regulator module (VRM)

Multi-core processors

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Today:

- Single off-chip voltage regulator module (VRM)
- One or more on-chip PLL clock generator modules

Multi-core processors

NICTA

Today:

- Single off-chip voltage regulator module (VRM)
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Per-core DVFS adds complexity to hardware and DVFS algorithms

How much energy can we really save?

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Up to now, we've ignored the performance loss...

We can:

How much energy can we really save?

NICTA

Up to now, we've ignored the performance loss...

We can:

- use a different benchmarking methodology;

How much energy can we really save?

NICTA

Up to now, we've ignored the performance loss...

We can:

- use a different benchmarking methodology;
- use a different metric;

How much energy can we really save?

NICTA

Up to now, we've ignored the performance loss...

We can:

- use a different benchmarking methodology;
- use a different metric;
- or both.

Padding methodology

Padding methodology

- Extend shorter executions;

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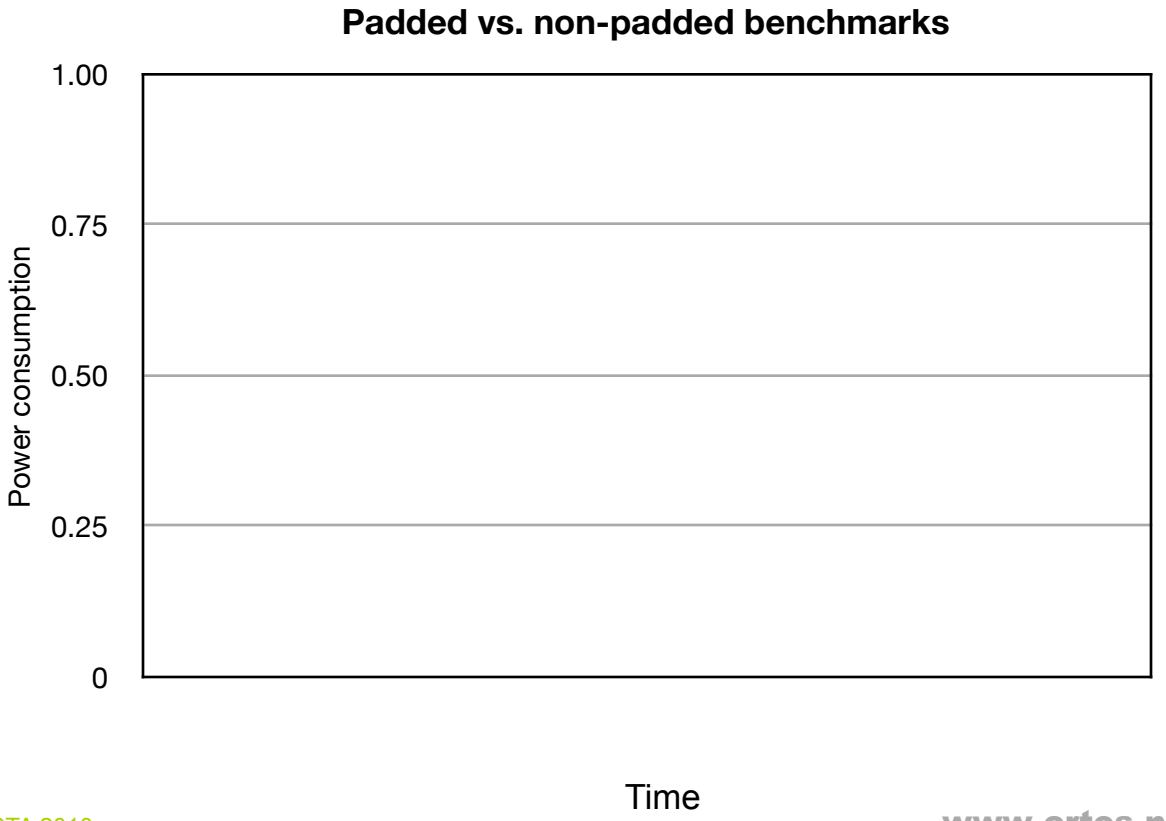

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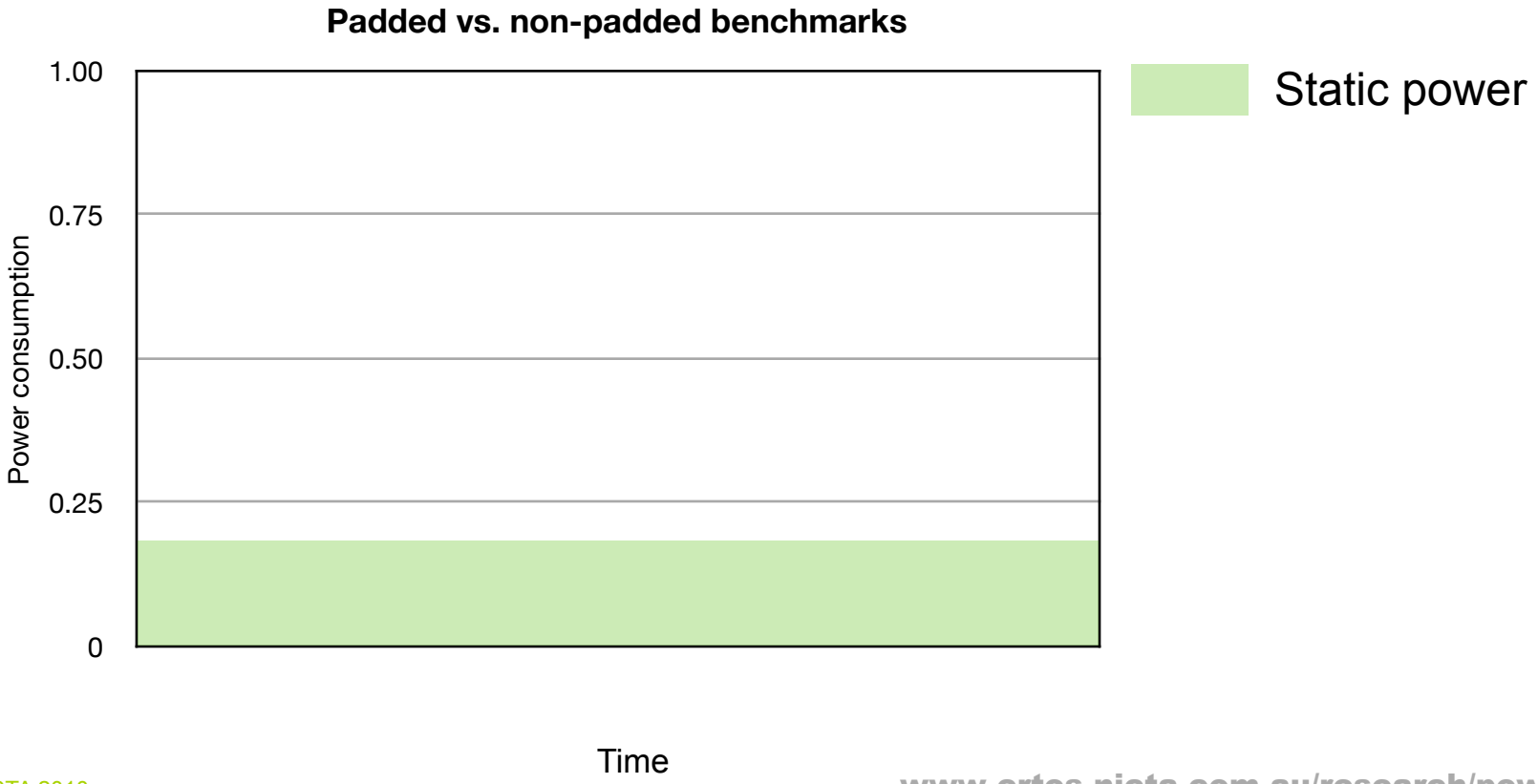

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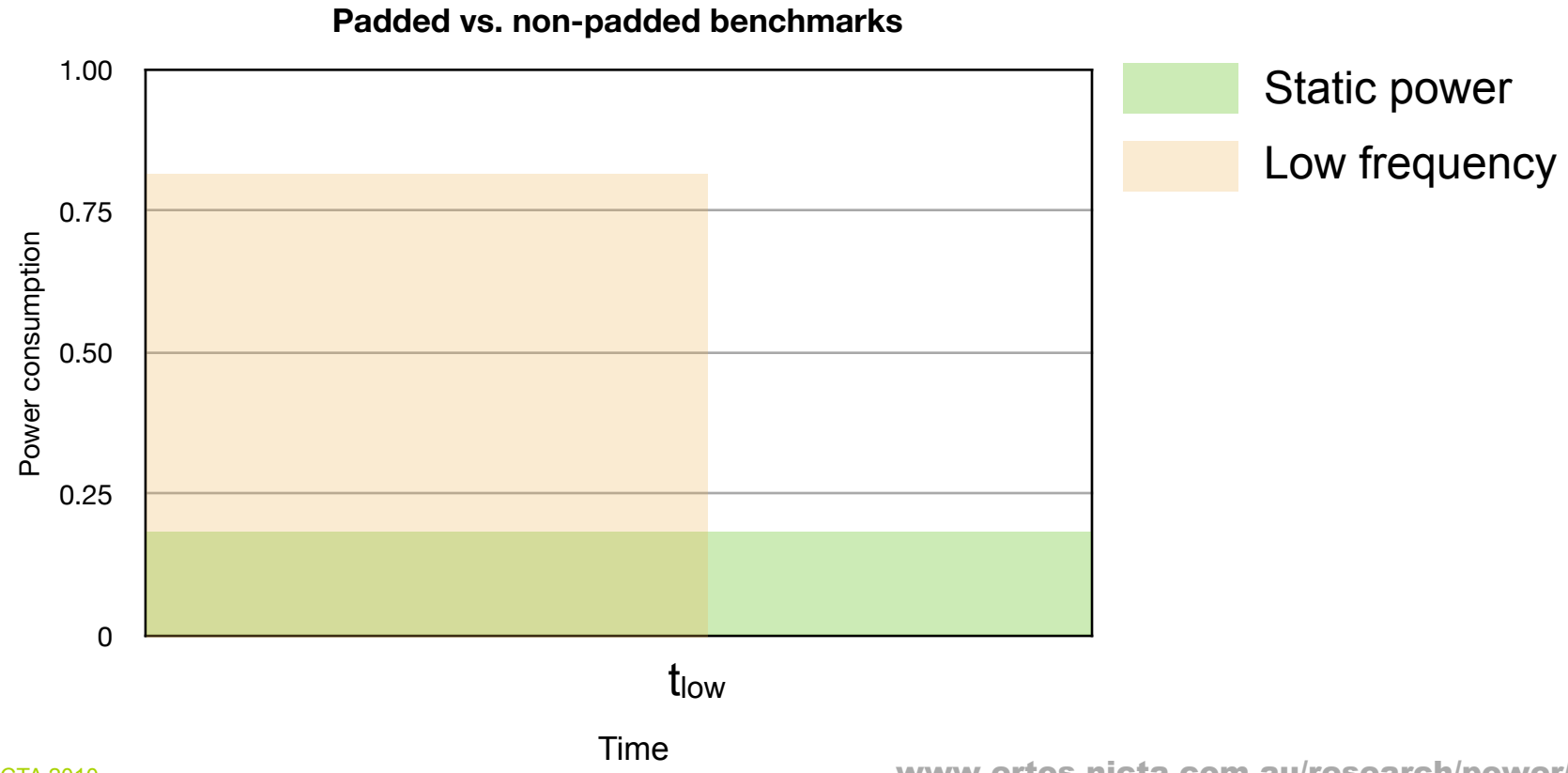

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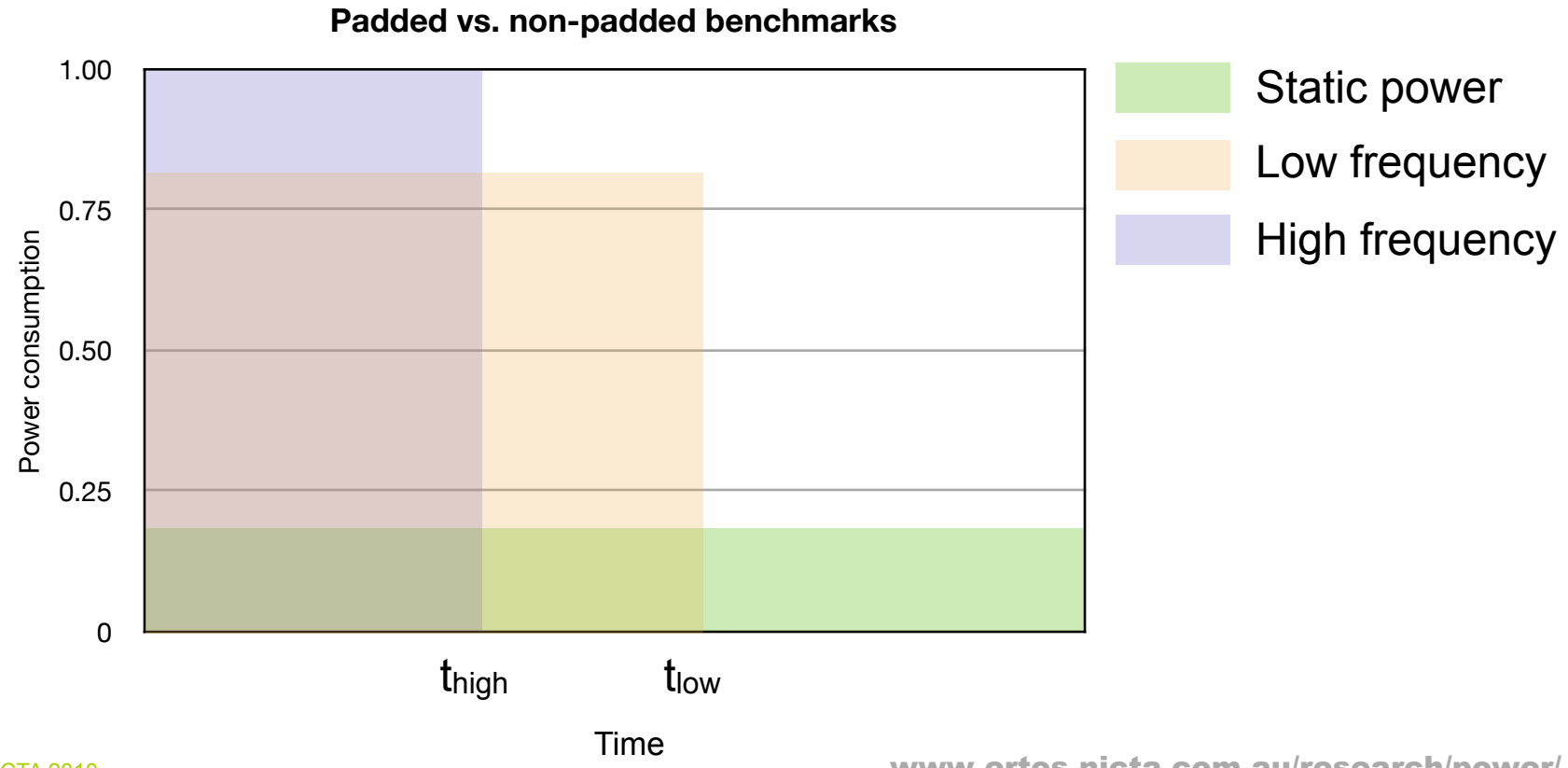

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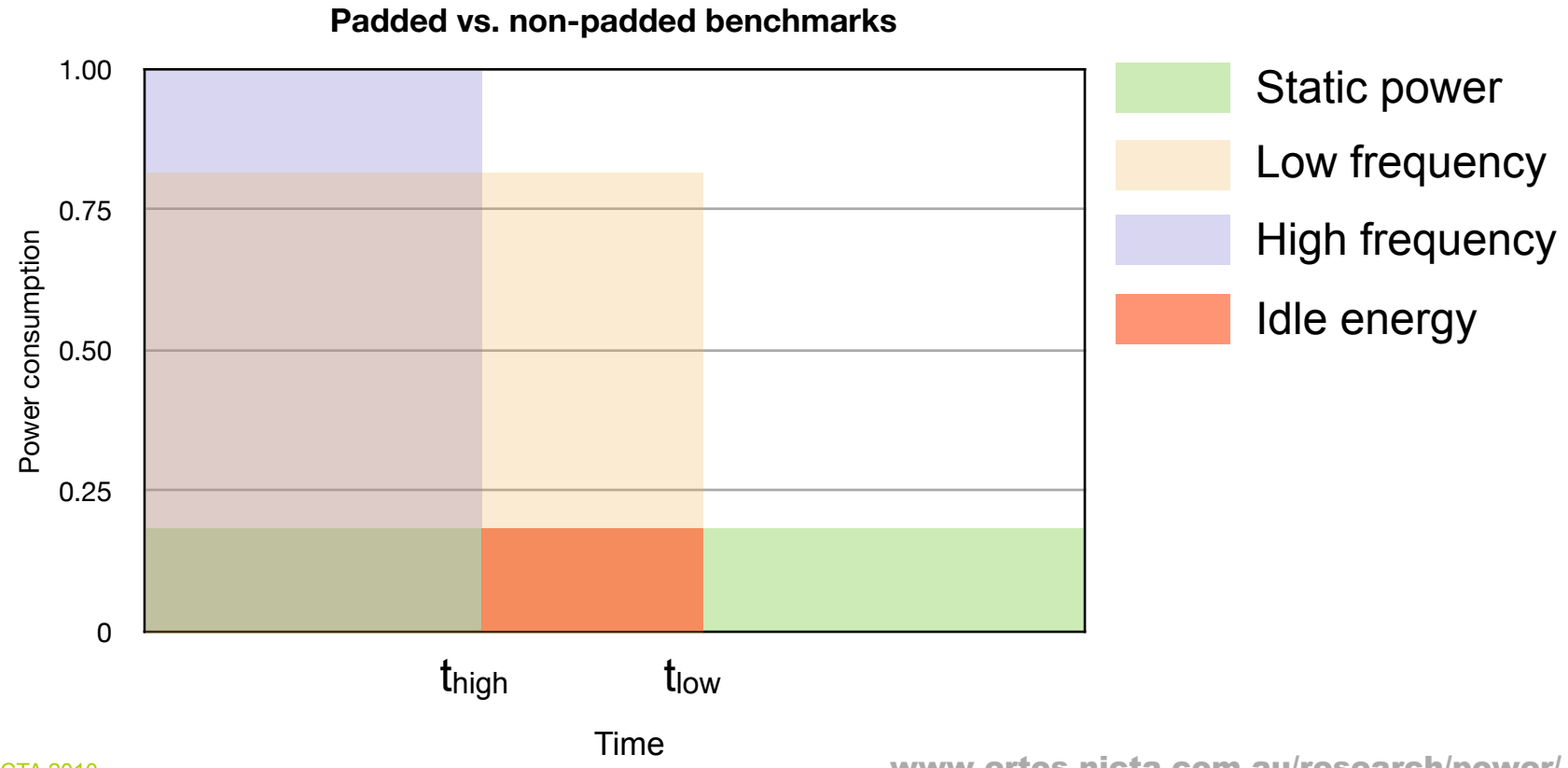

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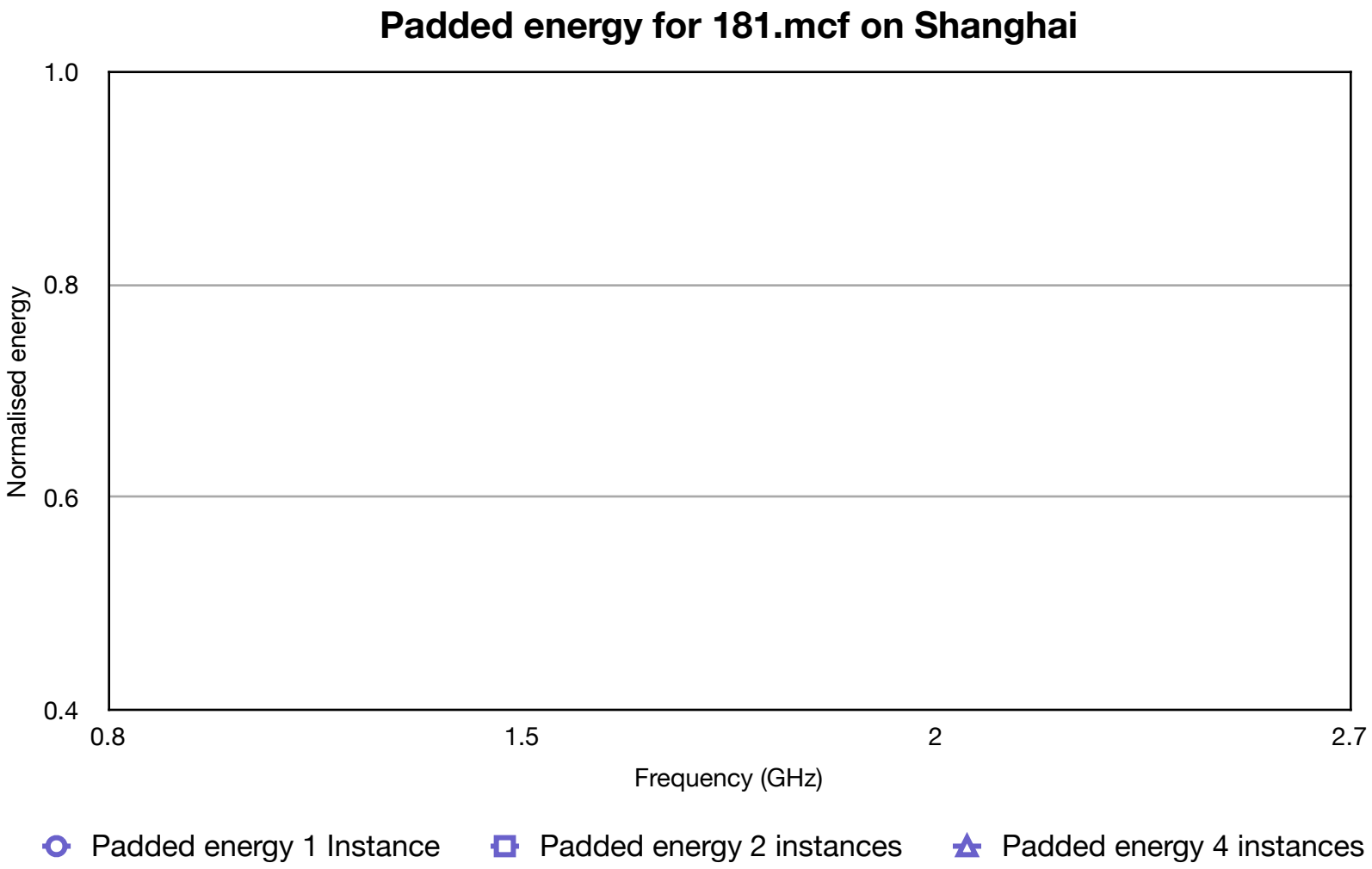

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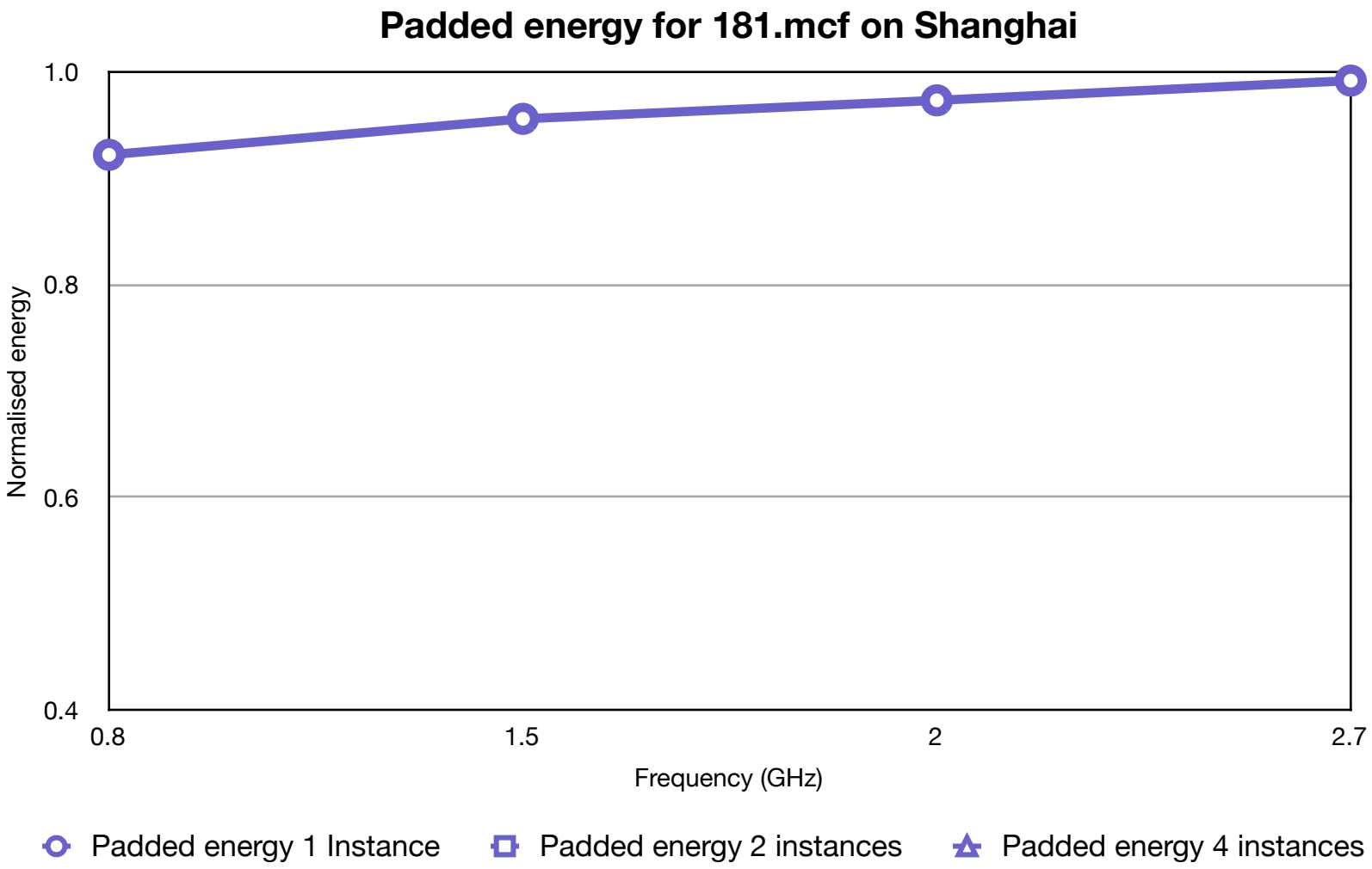

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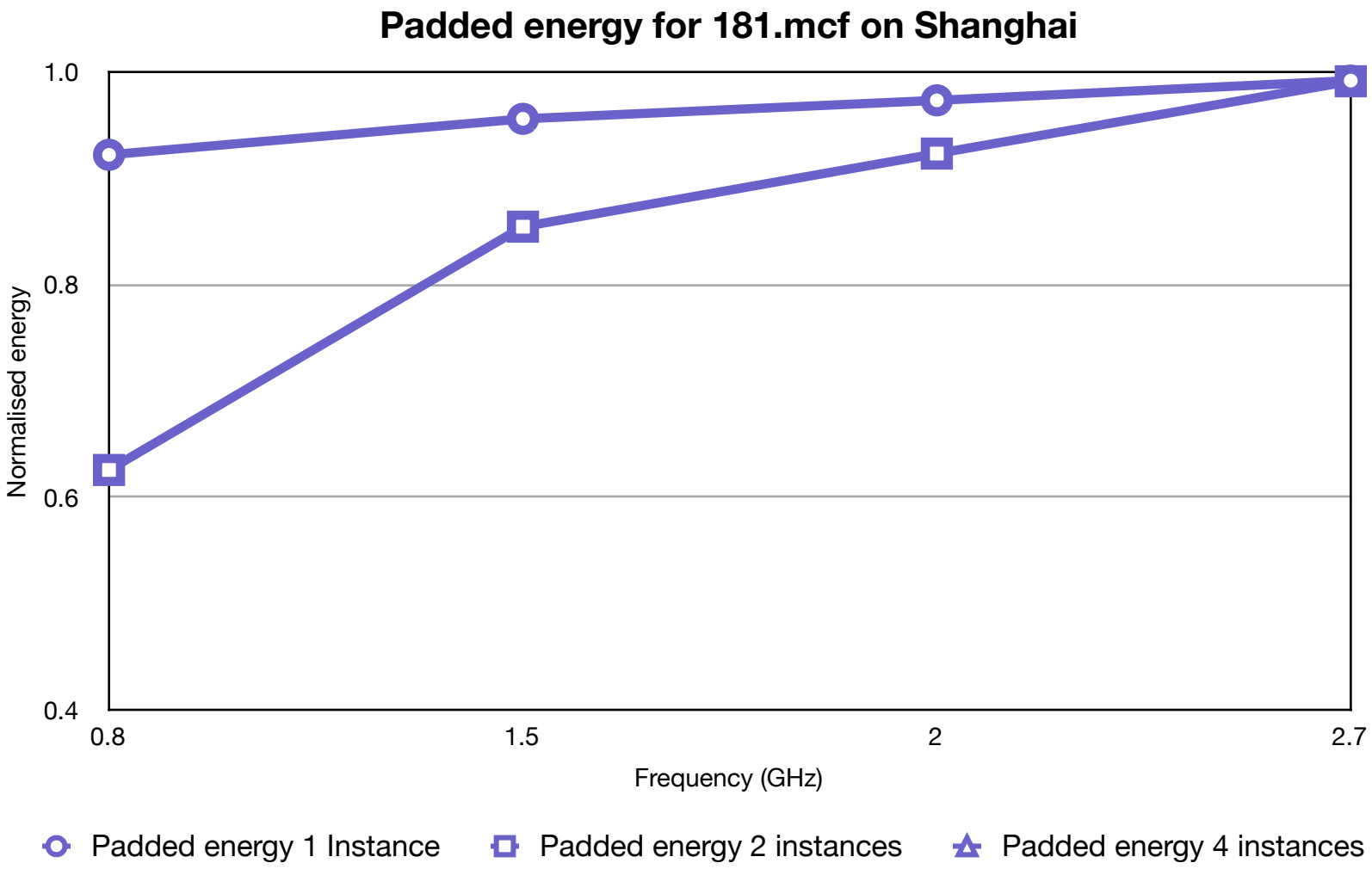

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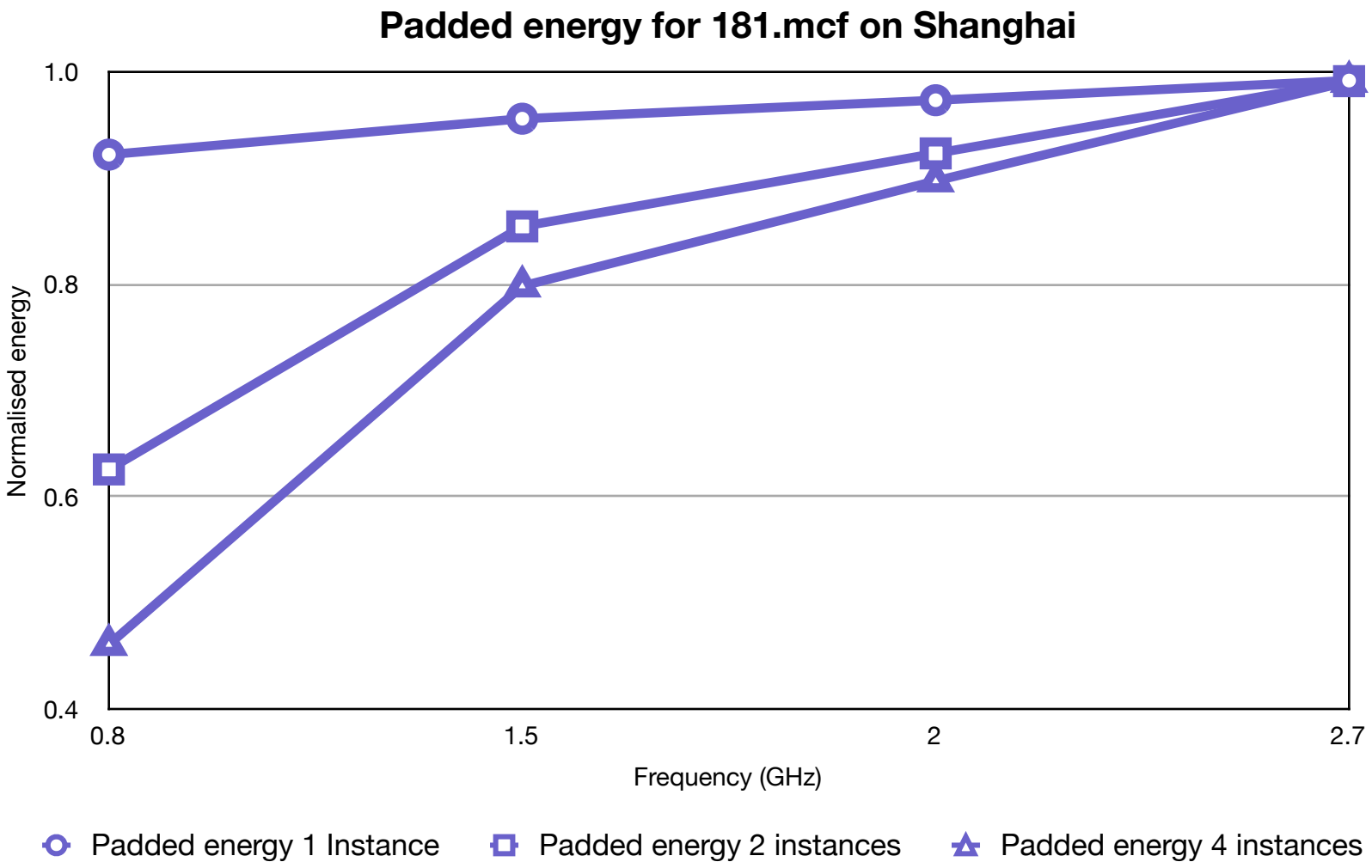

Padding methodology

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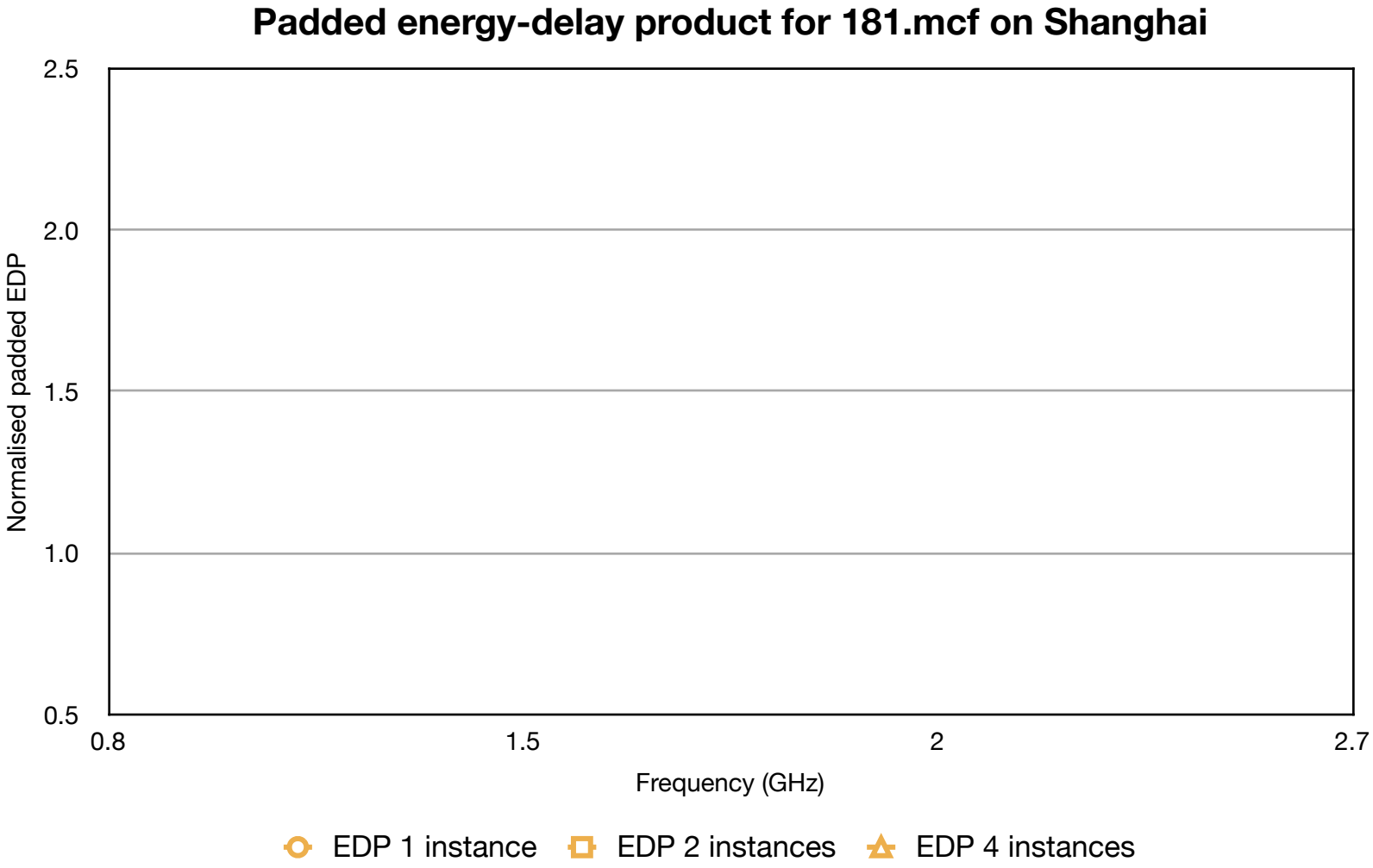
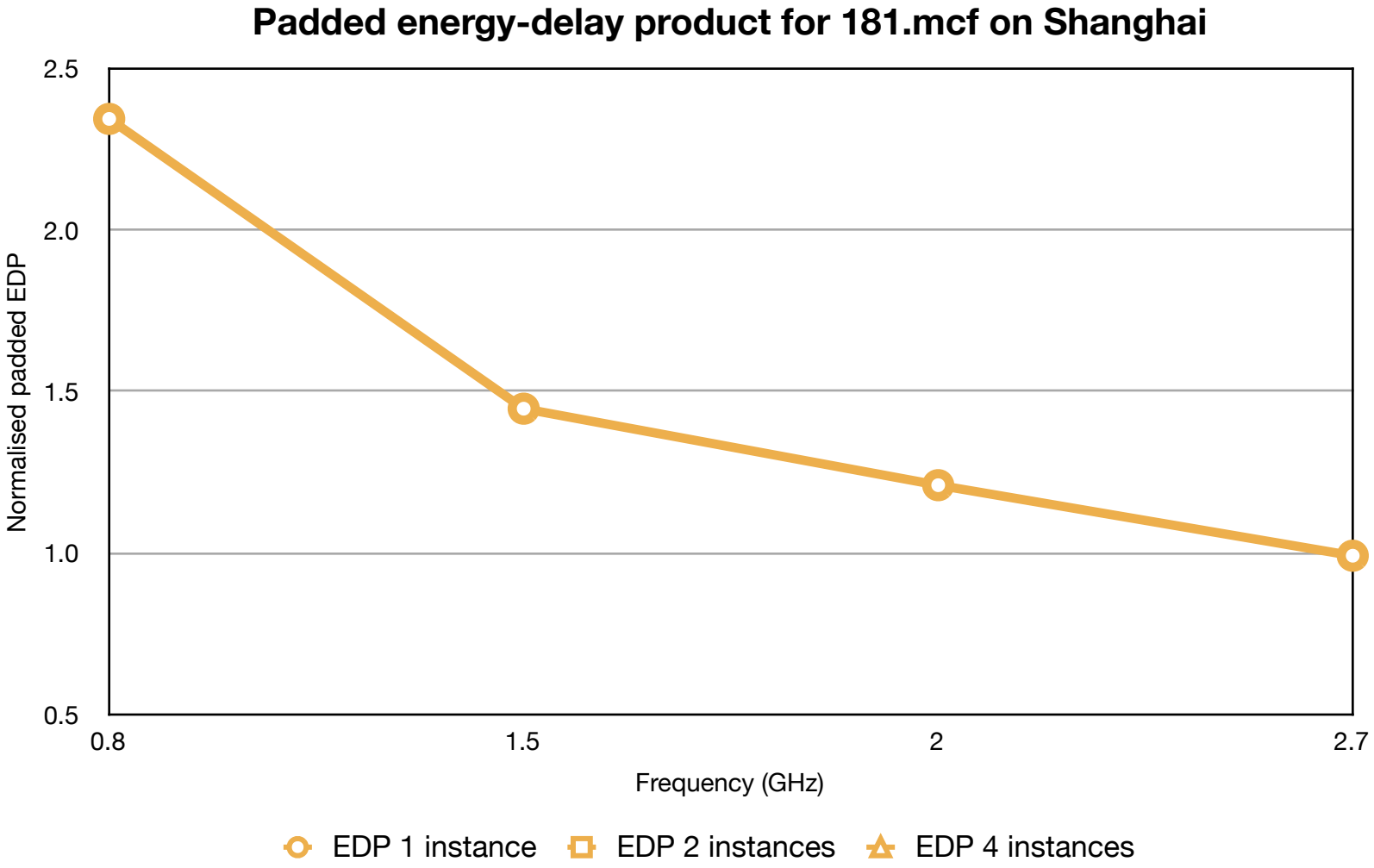
What about performance?

Energy-delay product

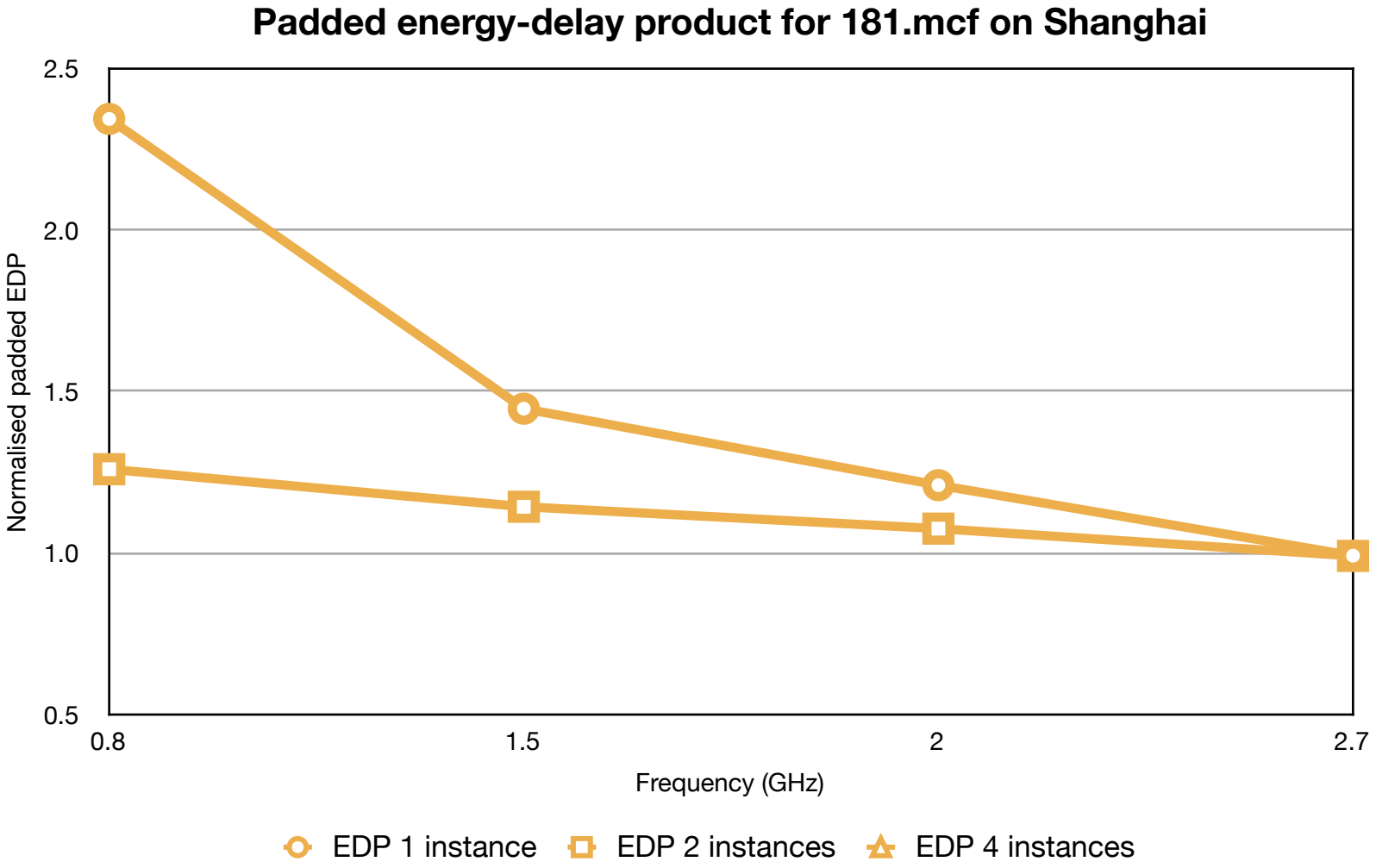
Energy-delay product



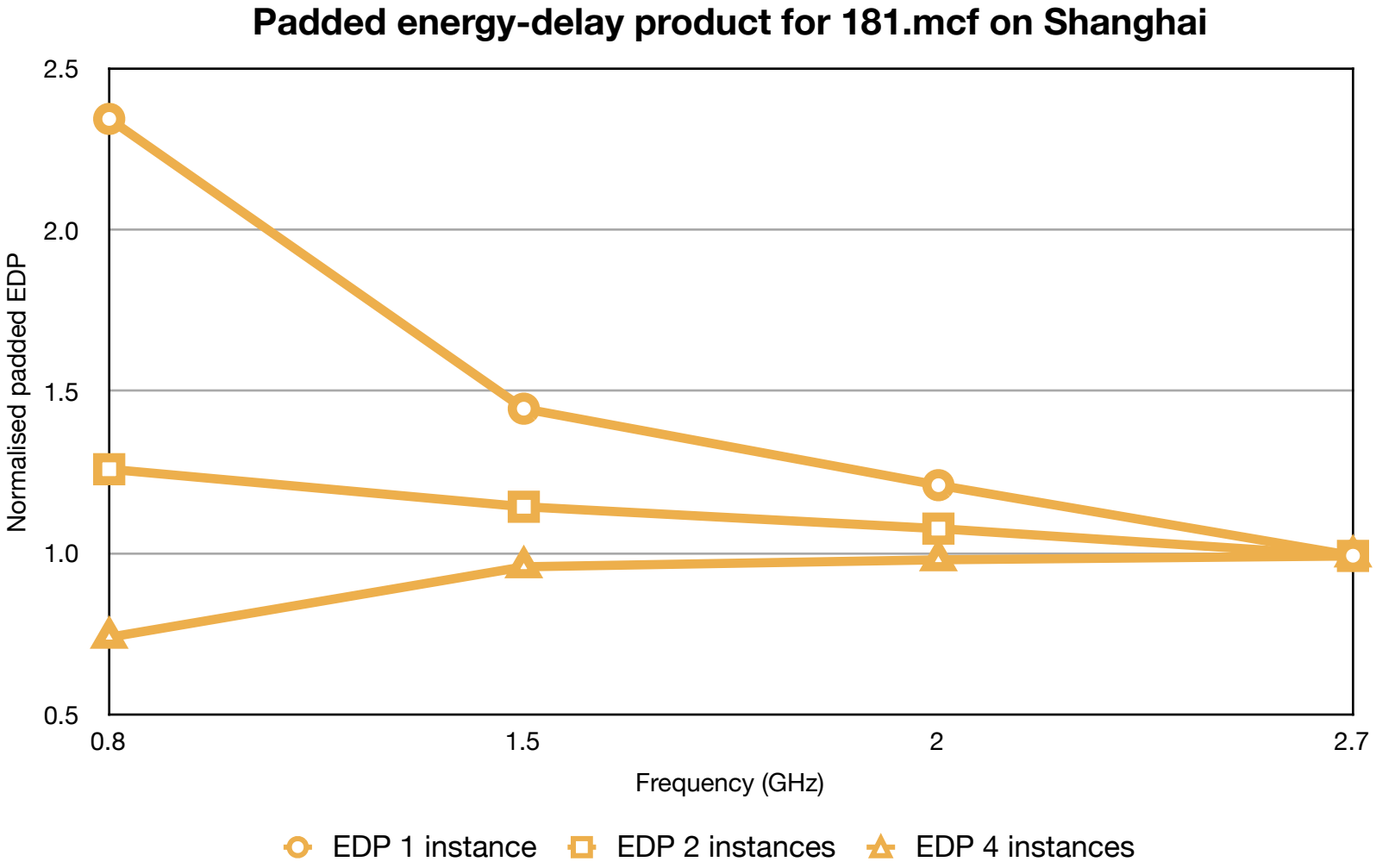
Energy-delay product



Energy-delay product



Energy-delay product



The future...

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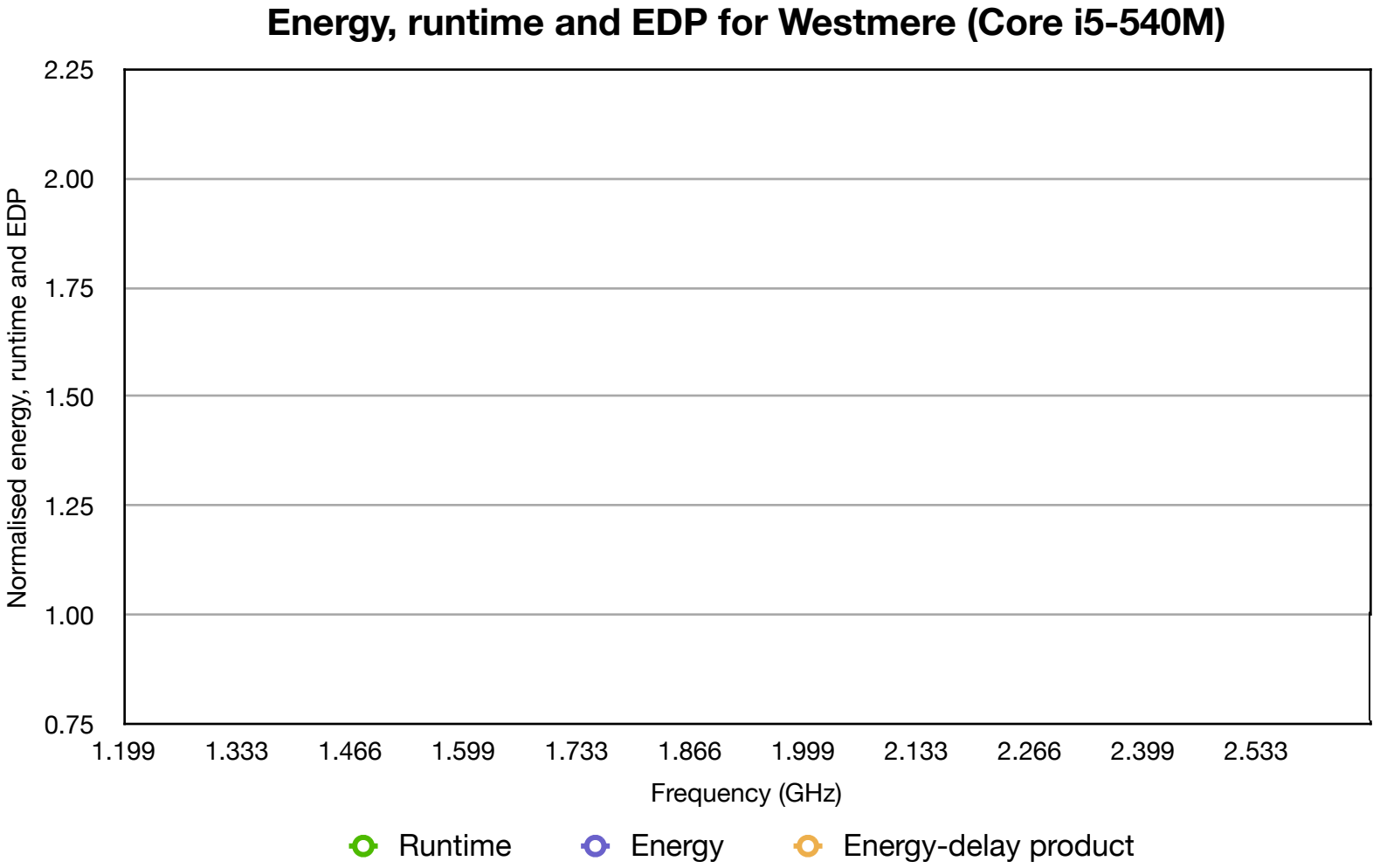
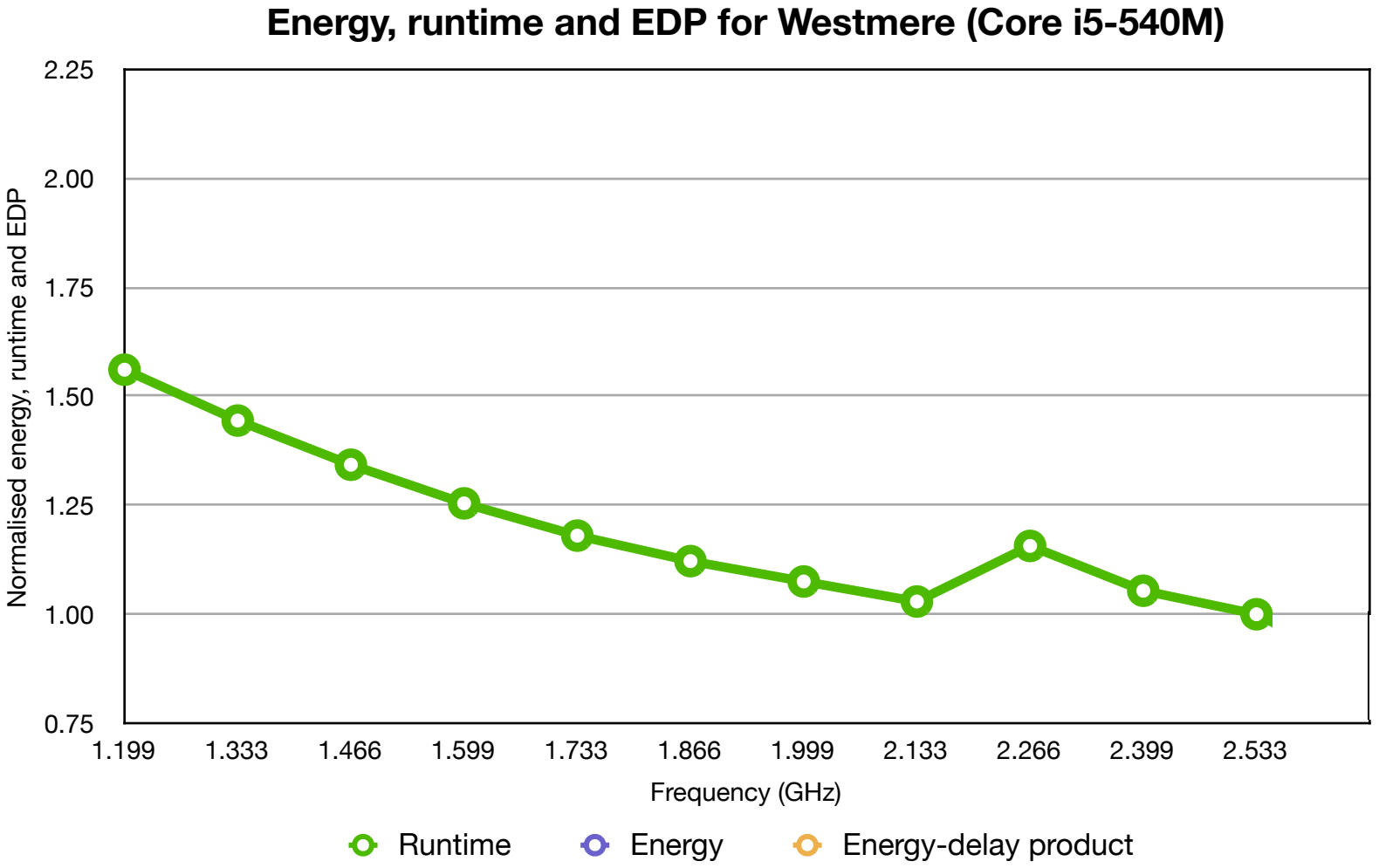
What about DVFS?

A glimpse

A glimpse



A glimpse



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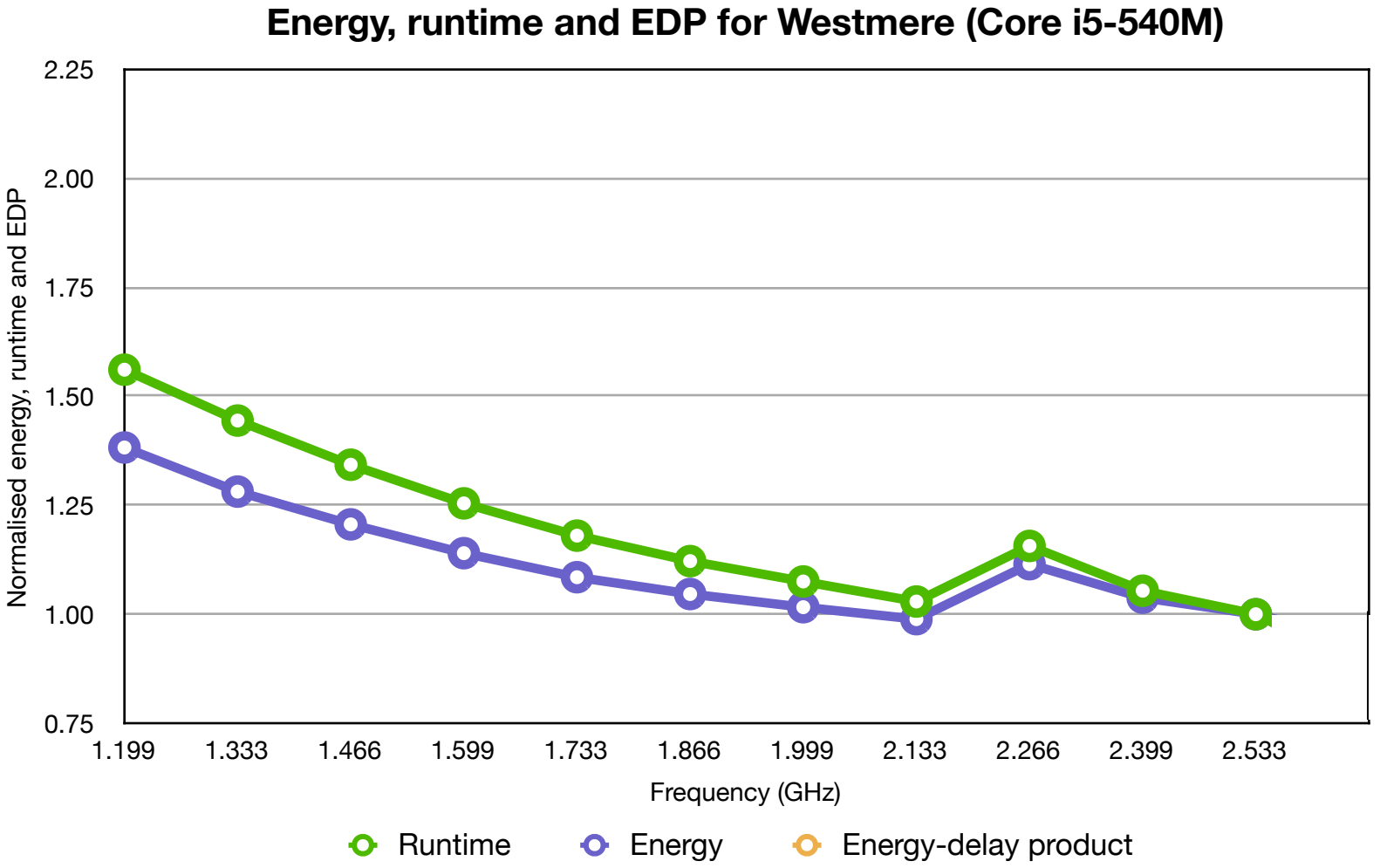

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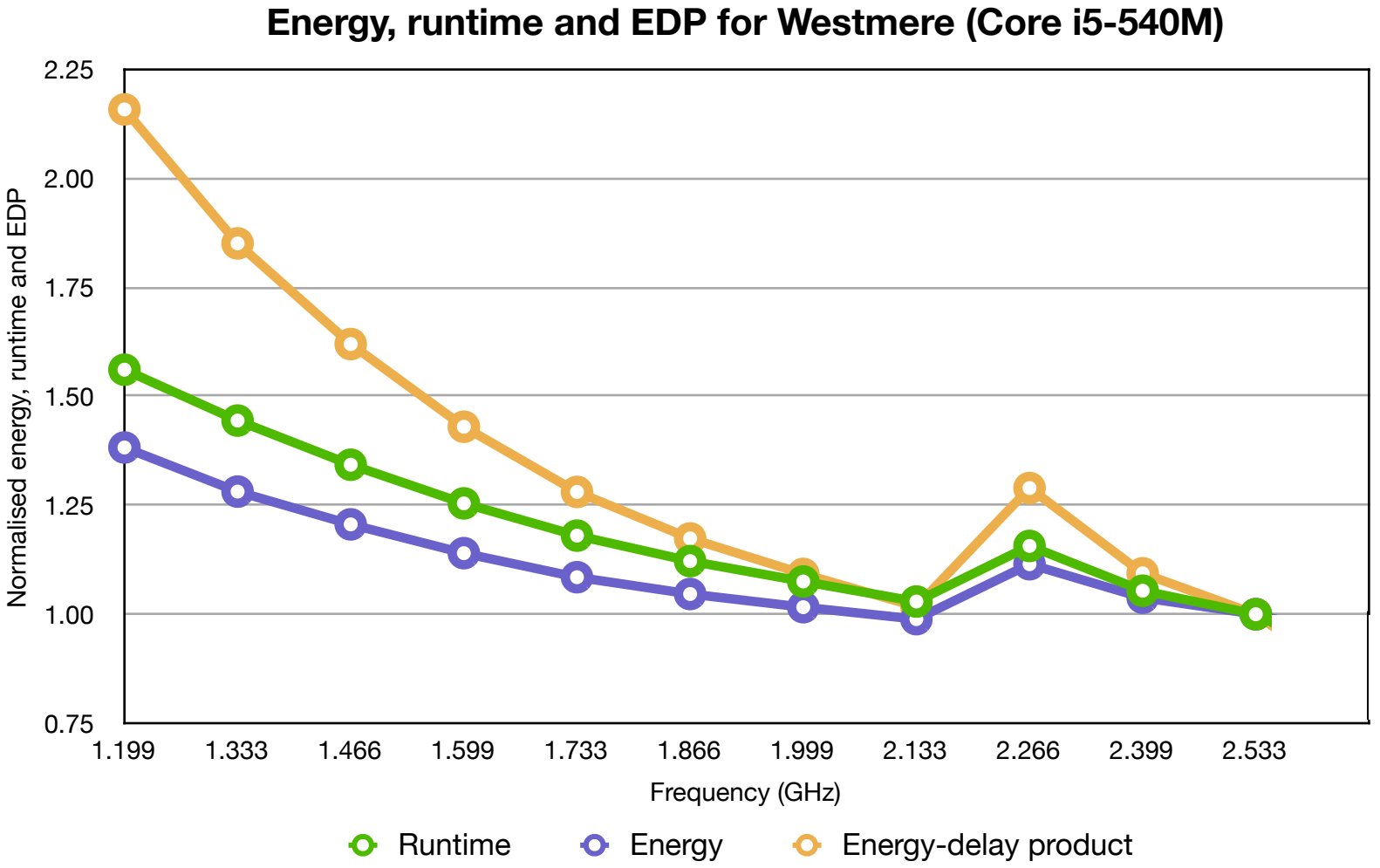

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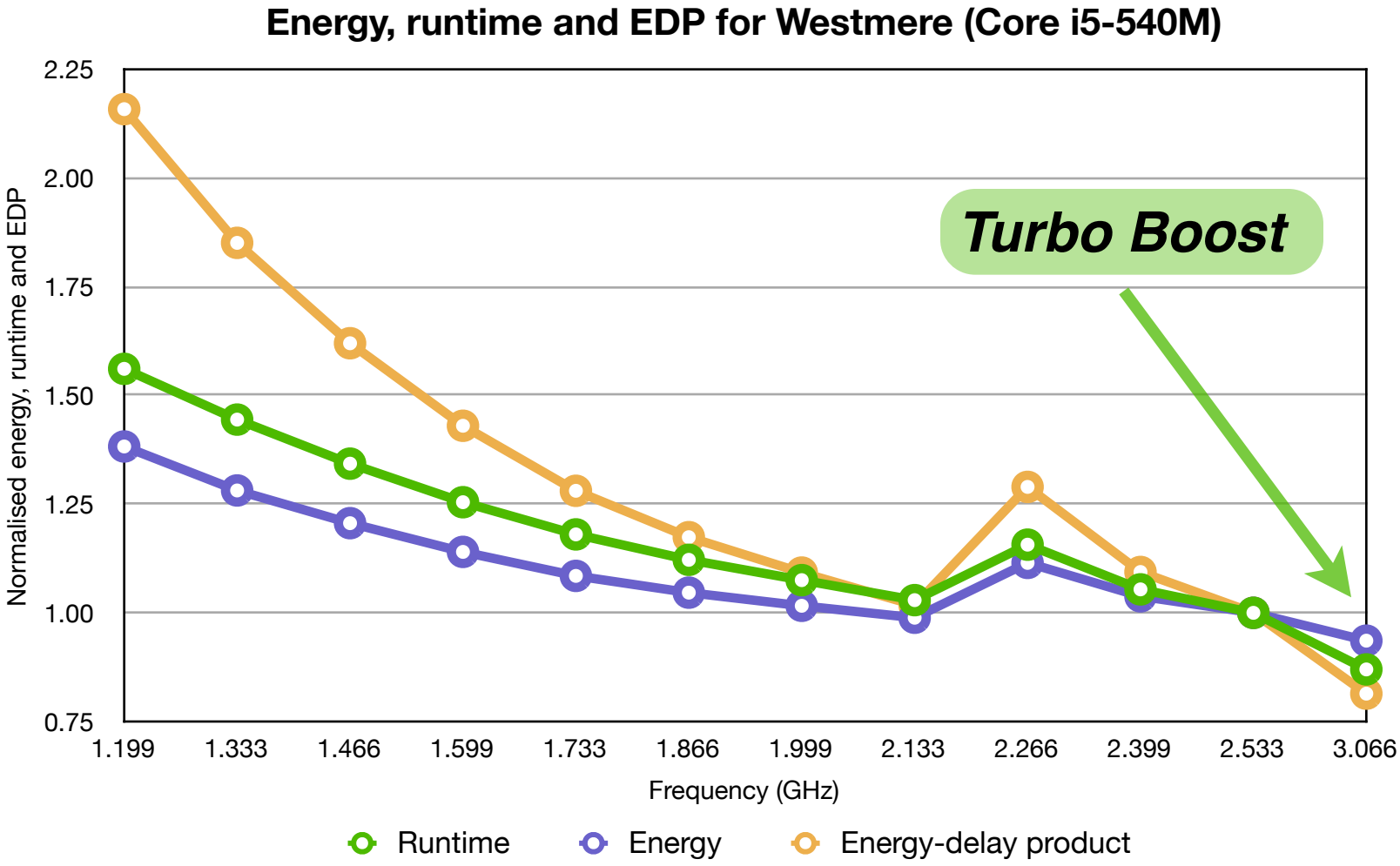

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Questions?

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Intel Atom N270

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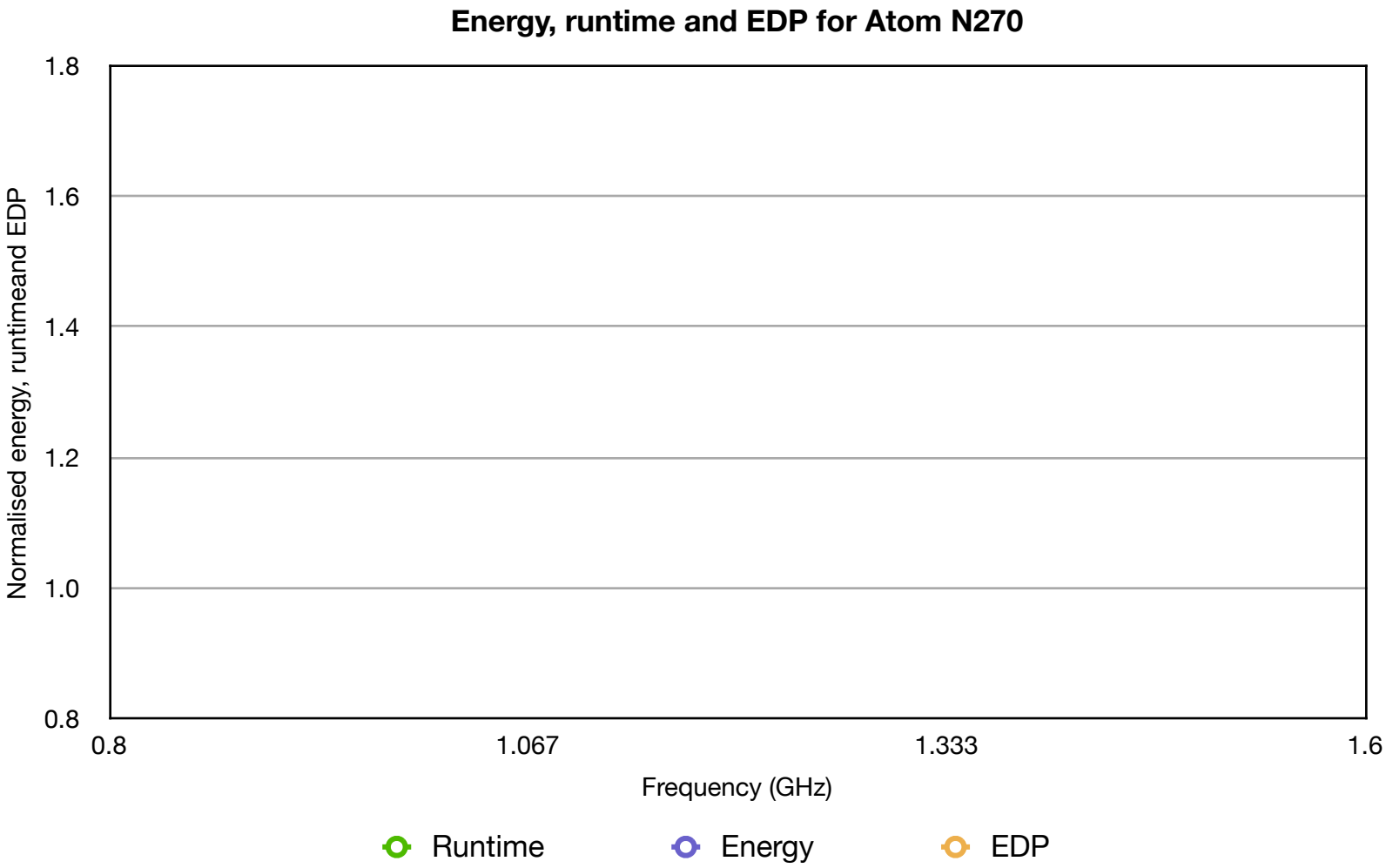
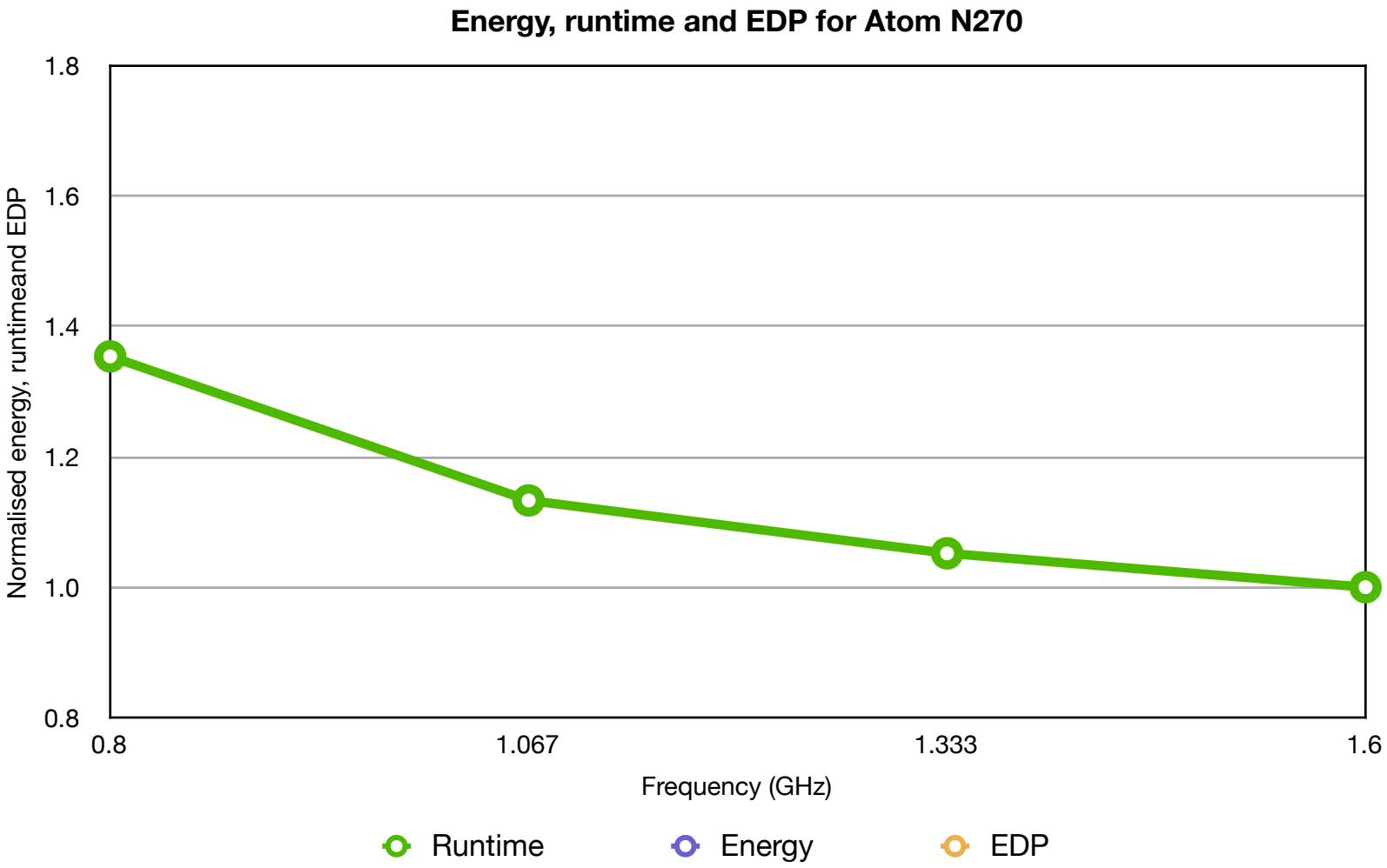
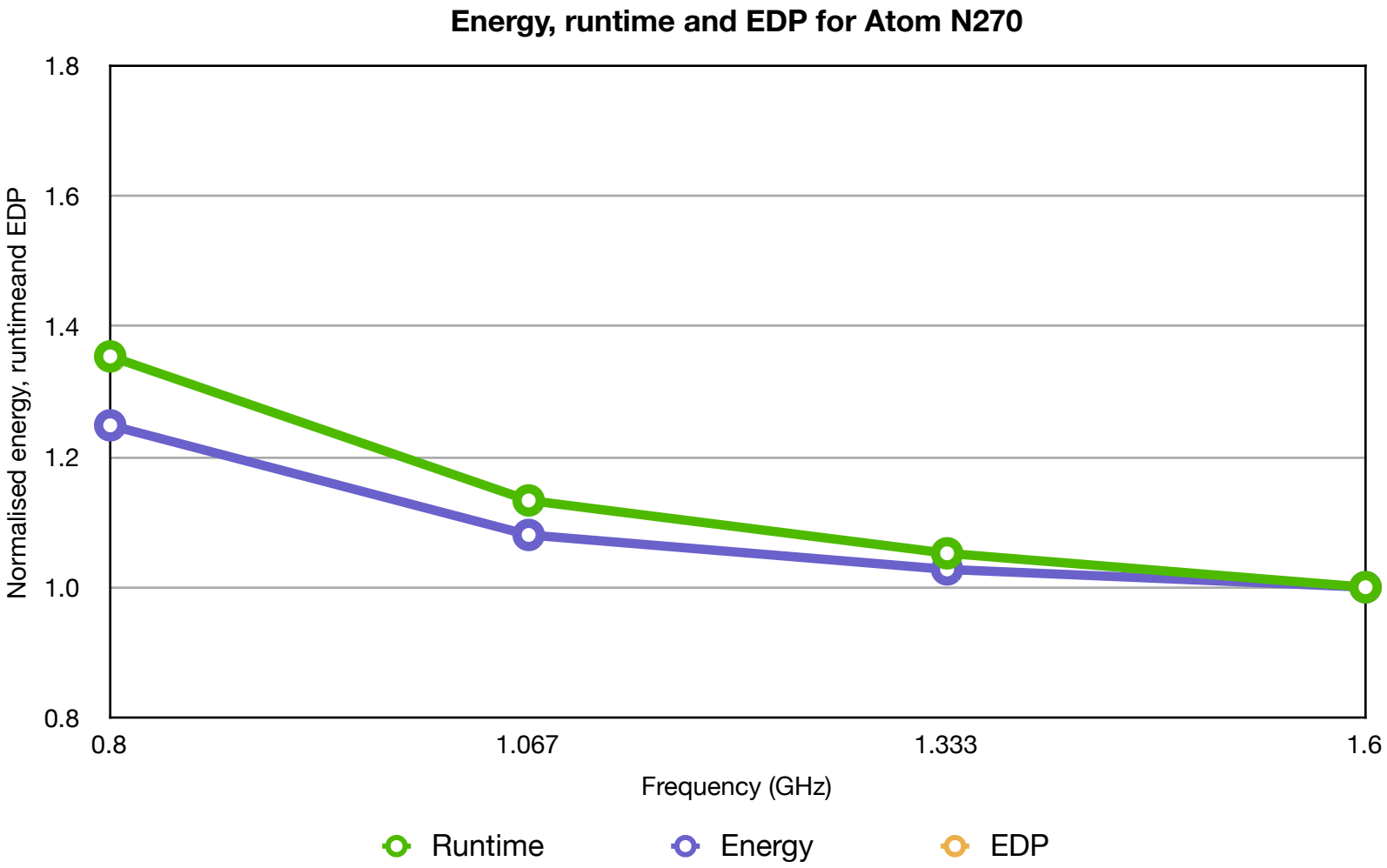


Intel Atom N270



Intel Atom N270



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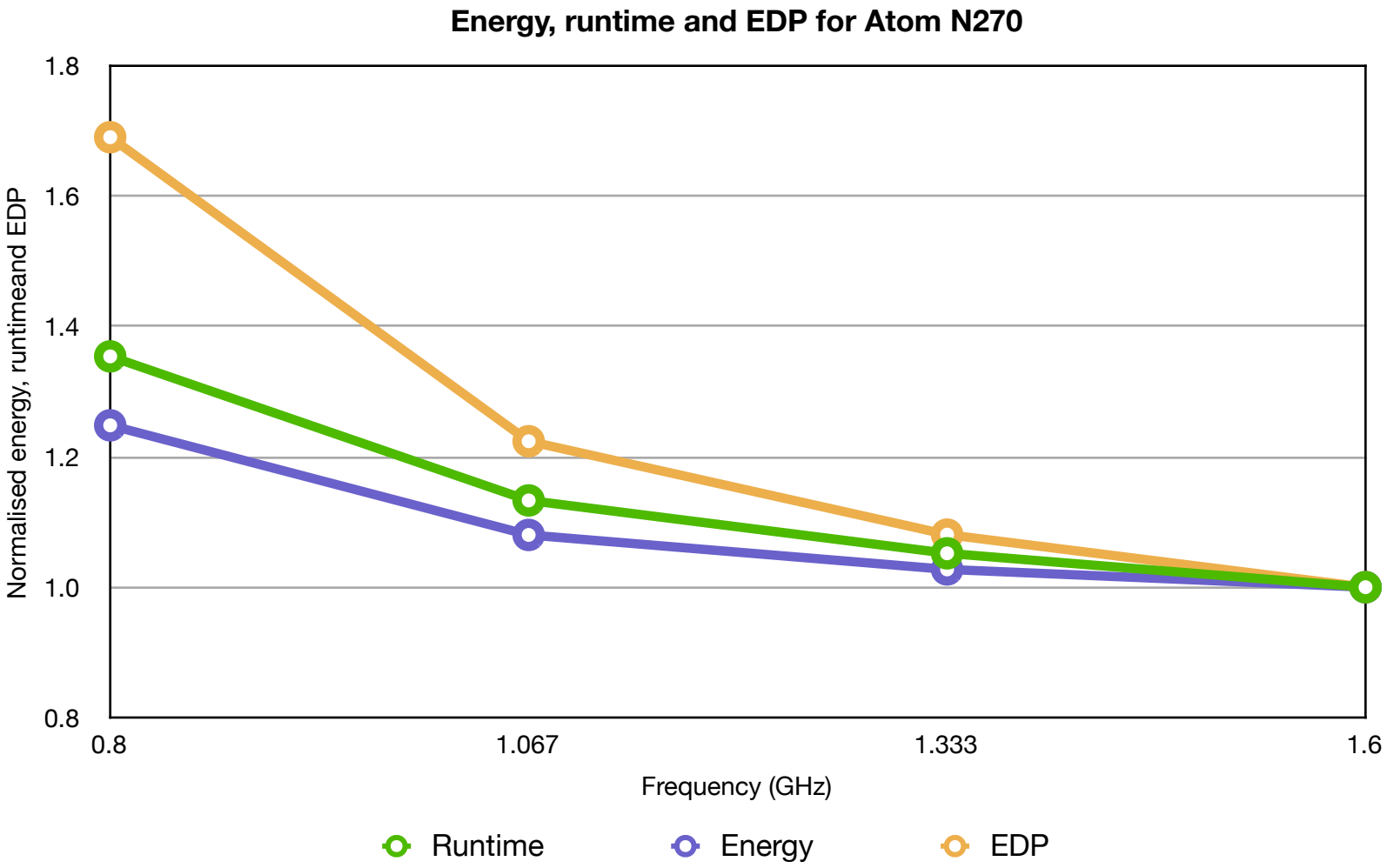
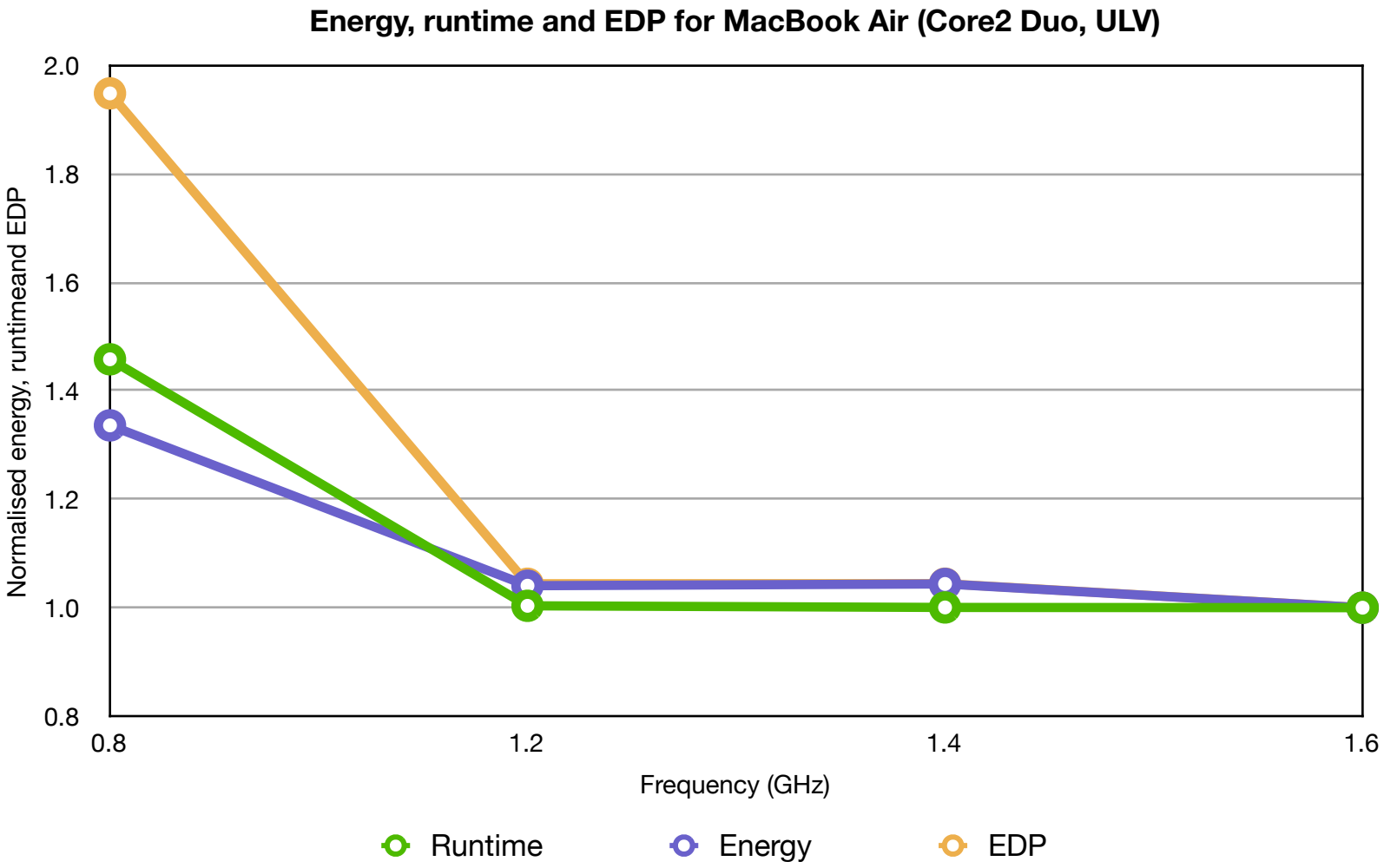


Intel Core 2 Duo (Ultra-low Voltage)




From imagination to impact

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