

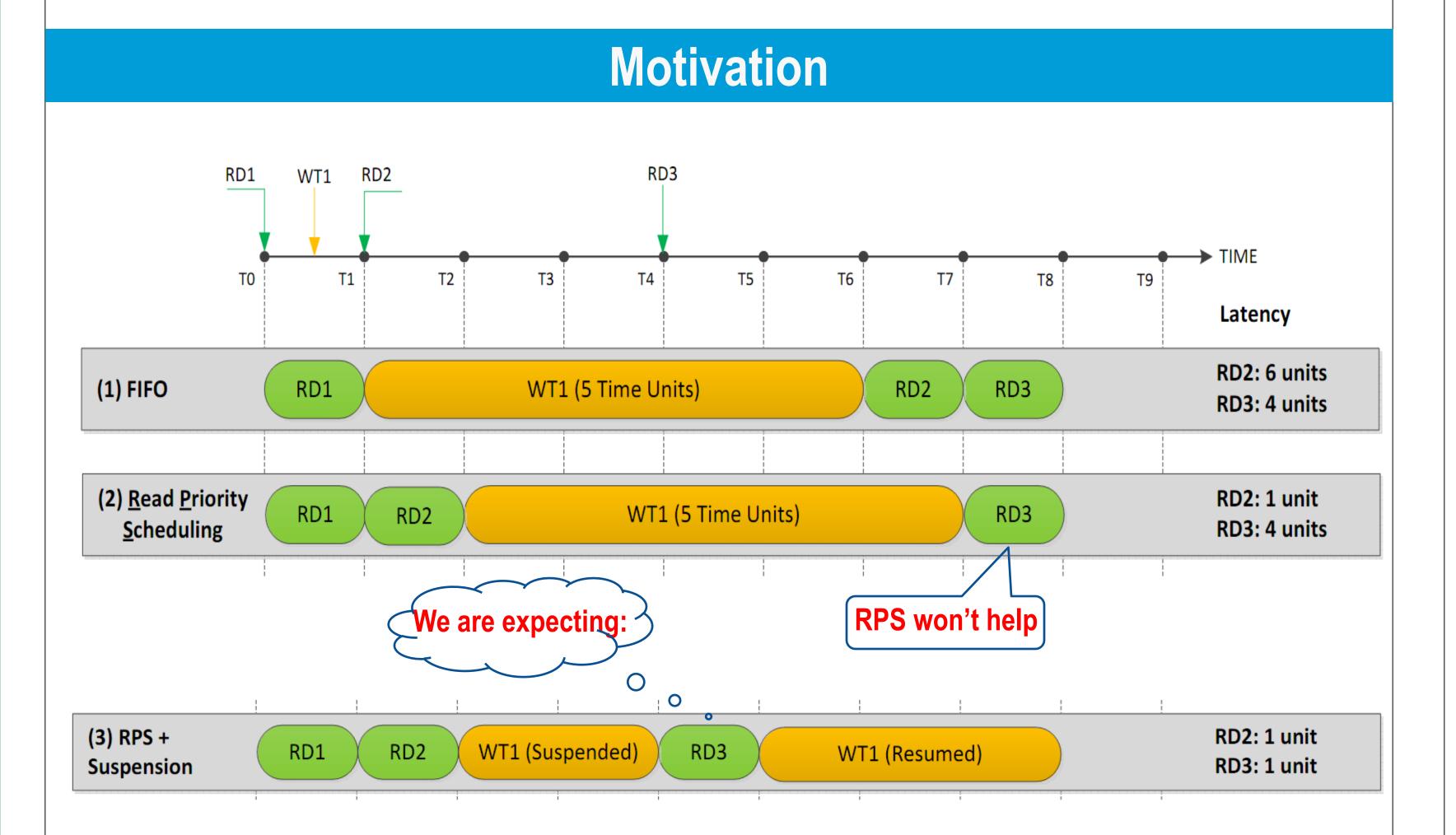
Reducing SSD Read Latency via NAND Flash Program and Erase Suspension

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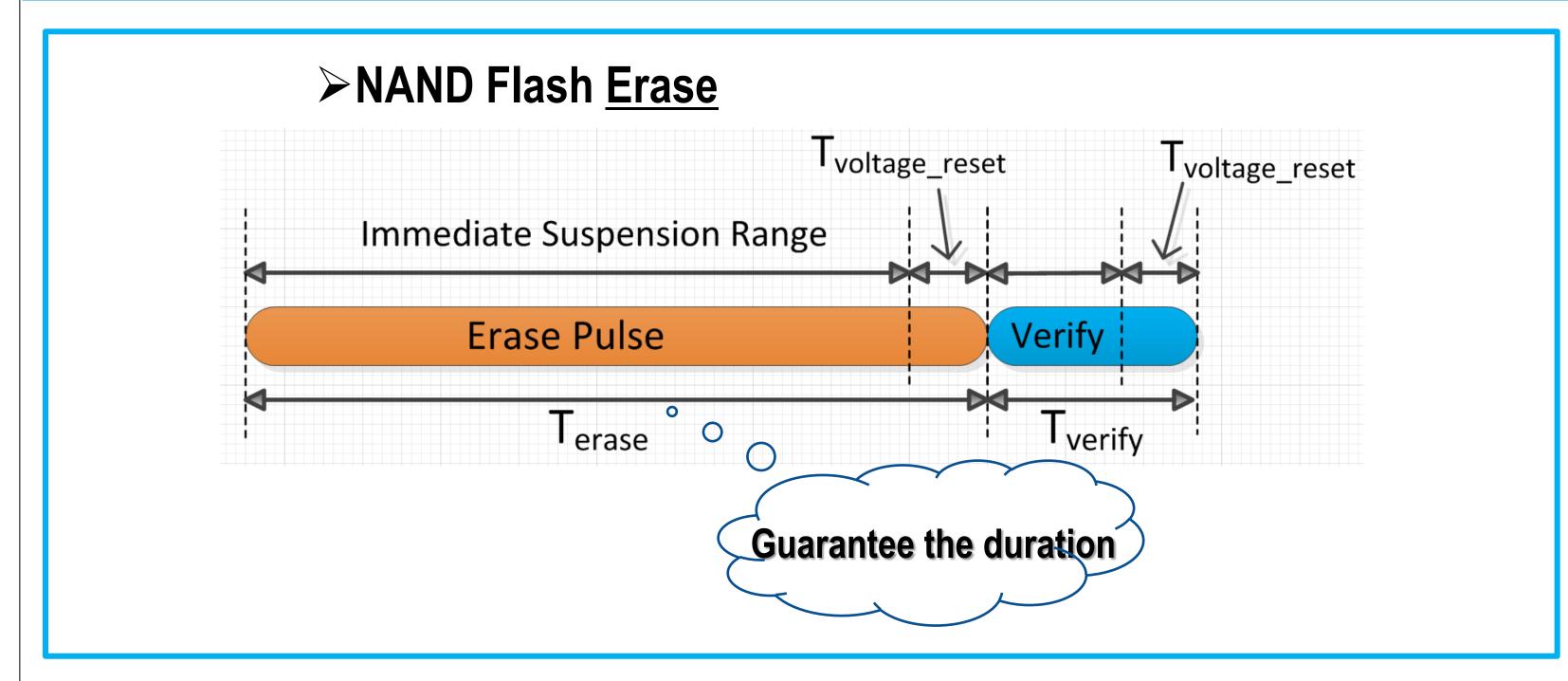
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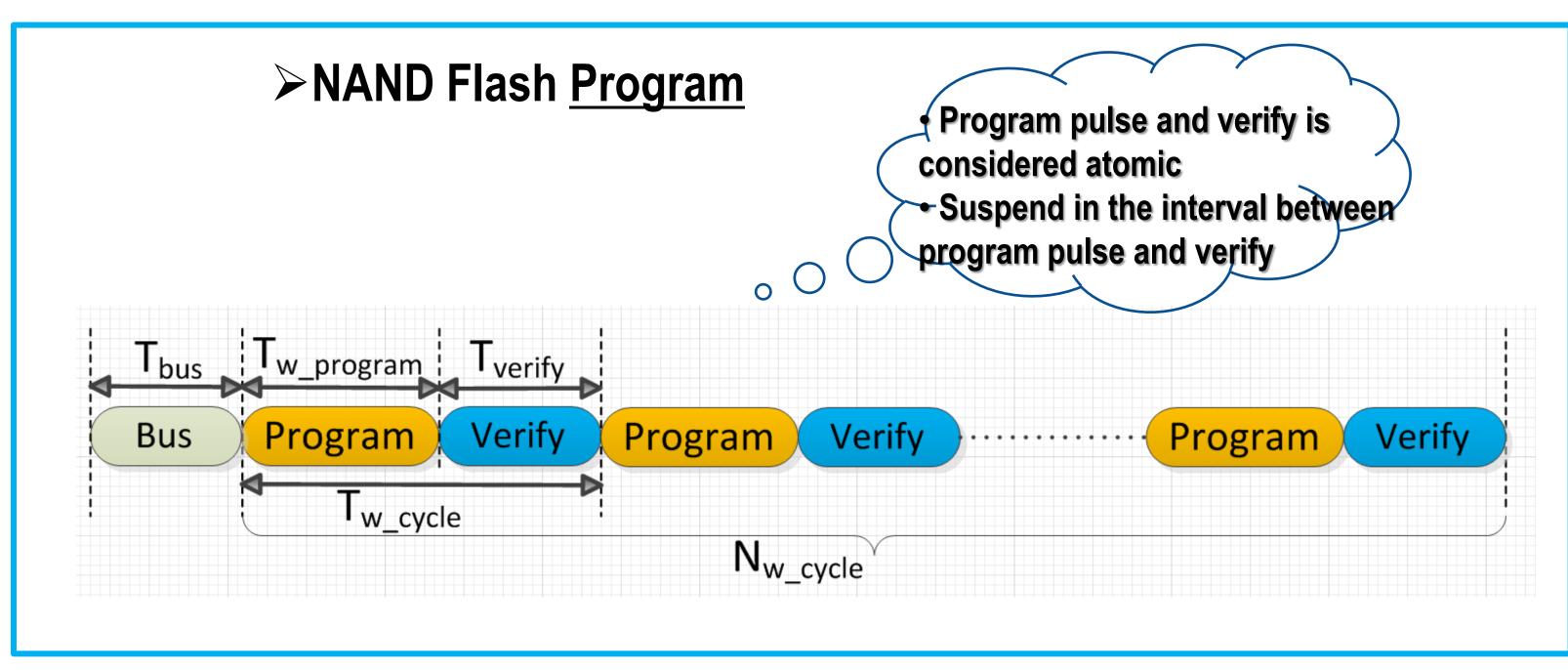
Introduction

In NAND flash memory, the program or erase (P/E) operations are non-suspendable. Therefore, the subsequent read requests have to wait until the time-consuming P/E operations to complete. This problem could increase the read latency by 2x. Inspired by the internal mechanism of NAND flash P/E algorithms, we propose a low-overhead P/E suspension scheme to reduce SSD read latency.



Background





References

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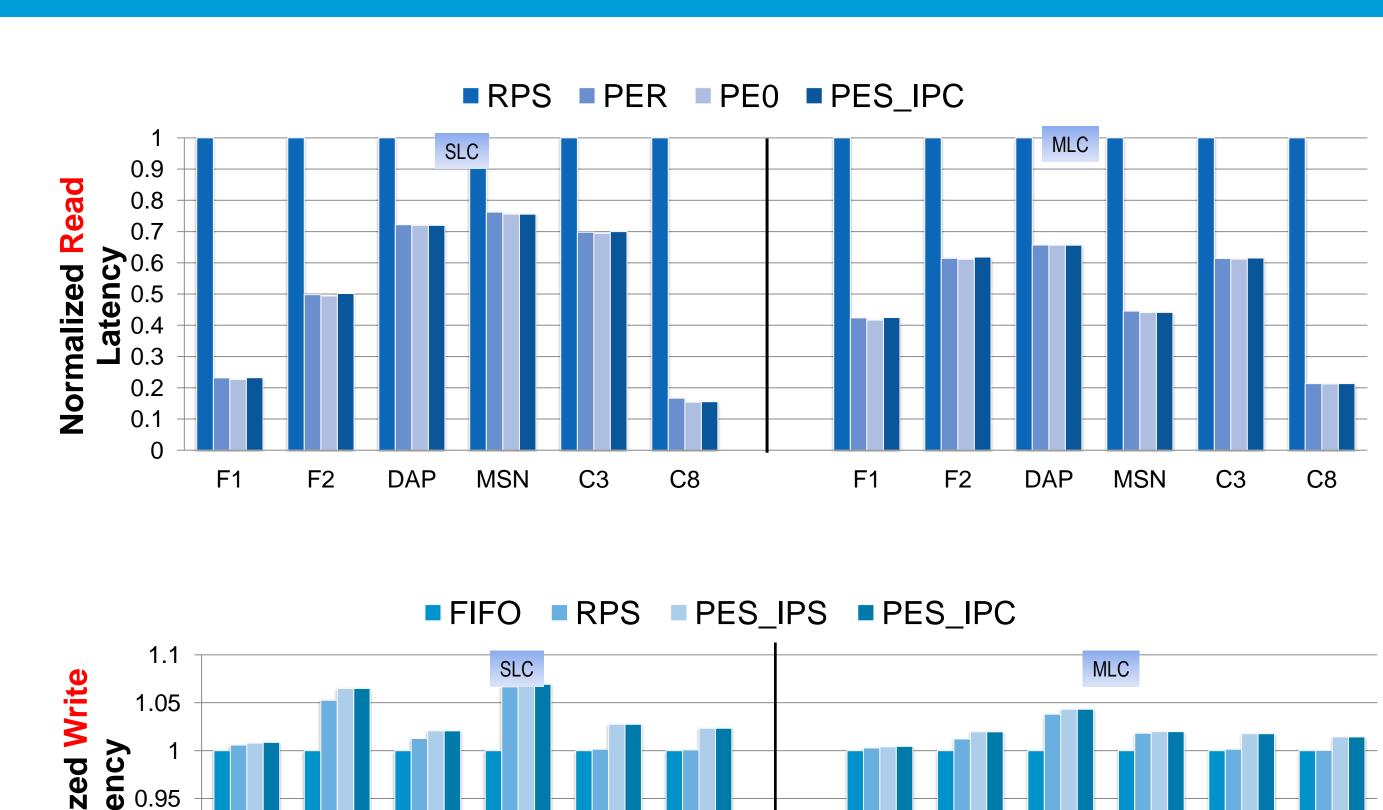
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Design >Suspend/Resume Erase □Case 1: Read arrives when resetting wire voltage voltage_reset Immediate Suspension Range **Erase Pulse** Suspension Point Read Arrival □Case 2: Read arrives at Immediate Suspension Range voltage_reset **Erase Pulse** Read **Suspension Point** Read Arrival >Suspend/Resume Erase □Case 1: Suspension happens at **Verify** phase ✓ Redo Verify phase. (overhead to erase latency) □Case 2: Suspension happens at **Erase** phase ✓ Finish what is left before suspension. >Suspend/Resume Program □Choice 1: Suspend in the intervals – Inter-Phase-Suspension Read Arrival Program Verify Program Verify Verify Program \ -Suspension Point Read Arrival Suspension Point □ Choice 2: Cancel the current phase – Intra-Phase-Cancellation Voltage reset P/V Cancelled Read Suspension Point >Suspend/Resume Program ☐Resume from **IPS** buffer

Resumption Point ☐ Resume from IPC Re-do PROG Buffer Verify Verify Resumption Point

Verify/Program



Evaluation

Buffer

Read

Read

Conclusion

- **■**Suspending P/E for read is achievable.
 - **✓** Easy to implement.
 - ✓ Significant read performance gain.
 - **✓ Low overhead on write latency.**

Program/Verify

(P/V cancelled)